APPLICATION NOTE

APPLICATION INFORMATION FOR PICTURE IN PICTURE CONTROLLER SAB9077 AN 96041

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Summary

The SAB 9077H in combination with two Multistandard decoders TDA 8310 and a memory of type D 482234 LE-70 (NEC) provides a Picture in Picture (PIP) system for the Multistandard environment.

It delivers one or two live video signals with reduced sizes for a live or frozen video signal.

Because of the two PIP-channels and a large external memory a wide range of PIP-modes are offered. The emphasis is put on double PIP and multi-PIP modes. In combination with an input video selector and some IIC-Bus software the SAB9077 system can be used e.g. as a channel selection tool.The hardware and software requirements for a good use of the SAB9077 are specified in this application note.

1 General Description

The SAB9077H is a picture in picture controller for Multi-standard TV-sets. The circuit contains Analog to Digital Converters, reduction circuitry, memory control, display control and Digital to Analog Convertors.

It inserts one or two live video signals with original or reduced sizes into a live video signal. All video signals are expected to be analog base band signals. The conversion into the digital environment and back to the analog environment is done on chip. Internal clocks are generated by two acquisition PLLs and a display PLL.

The two PIP channels and a large external memory offer a wide range of PIP modes. The emphasis is put on single PIP, double PIP, Split screen Mode and a many multi PIP modes.

2 Features

Display Features are:

- 50/60 Hz pip modes possible
- Twin PIP in interlaced mode at 8-bit resolution
- Sub-Title mode features built in
- Large Display Fine Positioning Area, both channels independent
- Only 2 MB needed as external VDRAM (2 x 1 MB or 1 x 2 MB)
- Four 8 bit AD converters (> 7-bit performance) with Clamp circuit
- Most PIP modes handle interlaced pictures without joint line error
- Two PLLs which generate the line locked clocks for the acquisition channels
- Display PLL to generate line locked clock for the display
- Three 8 bit DA converters
- 4:1:1 data format.
- Data reduction factors 1/1, 1/2, 1/3 and 1/4, horizontal and vertical independent

The following features are programmable via IIC:

- Single and Double PIP modes can be set
- Full Field Still Mode available
- Several aspect ratios can be handled
- Reduction factors can be set freely
- Selection of Vertical Filtering type
- Freeze of live pictures
- Fine tuned Display position, H (8 bit), V (8 bit), both channels independent
- Fine tuned Acquisition area, H (4 bit), V (8 bit), both channels independent
- Eight Main Border (Select), Sub Border (Select) and Background colors available
- Border and Background brightness adjustable, 30%, 50%, 70% and 100% IRE
- Several types of decoder input signals can be set

3 Package Outline

QFP100 (SOT317D8)

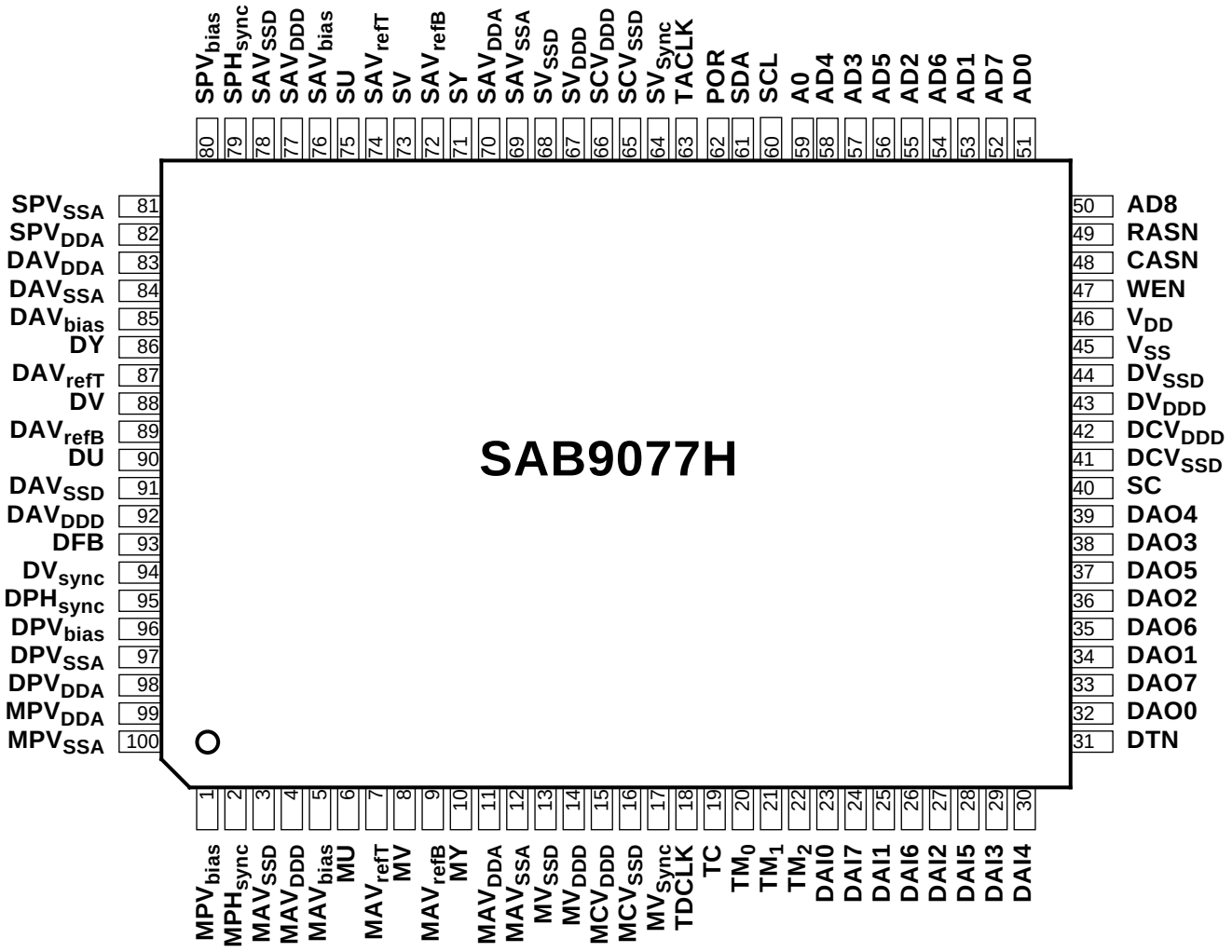

Figure 1: Pinning diagram of SAB9077H

4 Pinning

Symbol	Pin no.	I/O	Type	Description
SY	71	I	E027	Analog Y input of Sub Channel
SU	75	I	E027	Analog U input of Sub Channel
SV	73	I	E027	Analog V input of Sub Channel
SAV_{refT}	74	I	E027	Analog Top Reference for Sub Channel ADCs
SAV_{refB}	72	I	E027	Analog Bottom Reference of Sub Channel ADCs
SAV_{bias}	76	I/O	E027	Analog bias Reference of Sub Channel ADCs
SAV_{DDA}	70	I/O	E030	Analog V_{DD} of Sub Channel ADCs
SAV_{SSA}	69	I/O	E009	Analog V_{SS} of Sub Channel ADCs
SAV_{DDD}	77	I/O	E030	Digital V_{DD} of Sub Channel ADCs and PLLs
SAV_{SSD}	78	I/O	E009	Digital V_{SS} of Sub Channel ADCs and PLLs
SPH_{sync}	79	I	HPP01	Horizontal Sync Sub channel
SPV_{bias}	80	I/O	E027	Analog bias reference Sub Channel PLL
SPV_{DDA}	82	I/O	E030	Analog V_{DD} of Sub Channel PLL
SPV_{SSA}	81	I/O	E009	Analog V_{SS} of Sub Channel PLL
MY	10	I	E027	Analog Y input of Main Channel
MU	6	I	E027	Analog U input of Main Channel
MV	8	I	E027	Analog V input of Main Channel
MAV_{refT}	7	I	E027	Analog Top Reference for Main Channel ADCs
MAV_{refB}	9	I	E027	Analog Bottom Reference of Main Channel ADCs
MAV_{bias}	5	I	E027	Analog bias Reference of Main Channel ADCs
MAV_{DDA}	11	I/O	E030	Analog V_{DD} of Main Channel ADCs
MAV_{SSA}	12	I/O	E009	Analog V_{SS} of Main Channel ADCs
MAV_{DDD}	4	I/O	E030	Digital V_{DD} of Main Channel ADCs and PLLs
MAV_{SSD}	3	I/O	E009	Digital V_{SS} of Main Channel ADCs and PLLs
MPH_{sync}	2	I	HPP01	Horizontal Sync Main Channel
MPV_{bias}	1	I/O	E027	Analog bias reference Main Channel PLL
MPV_{DDA}	99	I/O	E030	Analog V_{DD} of Main Channel PLL
MPV_{SSA}	100	I/O	E009	Analog V_{SS} of Main Channel PLL
SV_{sync}	64	I	HPP01	Vertical sync Sub Channel
MV_{sync}	17	I	HPP01	Vertical sync Main Channel
DV_{sync}	94	I	HPP01	Vertical sync Display channel
SDA	61	I/O	IOI41	Shift in data IIC bus, ACK out IIC bus
SCL	60	I	HPF01	Shift clock for IIC bus
A0	59	I	HPF01	IIC address select pin
POR	62	I	HUP07	Power on Reset
TM(2)	22	I/O	HOU21	Test Mode pin, Input level selection
$TM_{(1:0)}$	21/20	I	HPP01	Test mode pins
TC	19	I	HPP01	Test Control
TDCLK	18	I	HPP01	Test Clock Display
TACLK	63	I	HPP01	Test Clock Acquisition

SC	40	O	OPF20	Memory Shift Clock
DTN	31	O	OPF20	Memory Data Transfer
WEN	47	O	OPF20	Memory Write Enable
CASN	48	O	OPF20	Memory Column Address Strobe
RASN	49	O	OPF20	Memory Row Address strobe
DAI(7:0)	23-30	I	HPP01	Memory to SAB9077H input data bus (7:0)
DAO(7:0)	32-39	O	OPF20	SAB9077H to Memory output data bus (7:0)
AD(8:0)	50-58	O	OPF20	Memory address bus (8:0)
SV_{DDD}	67	I/O	E030	Digital V_{DD} Sub Channel Core
SV_{SSD}	68	I/O	E009	Digital V_{SS} Sub Channel Core
MV_{DDD}	14	I/O	E030	Digital V_{DD} Main Channel Core
MV_{SSD}	13	I/O	E009	Digital V_{SS} Main Channel Core
DV_{DDD}	43	I/O	E030	Digital V_{DD} Display Core
DV_{SSD}	44	I/O	E009	Digital V_{SS} Display Core
V_{DD}	46	I/O	E030	Digital V_{DD} Periphery
V_{SS}	45	I/O	E009	Digital V_{SS} Periphery
SCV_{DDD}	66	I/O	E030	Digital V_{DD} of Sub Clock buffer
SCV_{SSD}	65	I/O	E009	Digital V_{SS} of Sub Clock buffer
MCV_{DDD}	15	I/O	E030	Digital V_{DD} of Main Clock buffer
MCV_{SSD}	16	I/O	E009	Digital V_{SS} of Main Clock buffer
DCV_{DDD}	42	I/O	E030	Digital V_{DD} of Display Clock buffer
DCV_{SSD}	41	I/O	E009	Digital V_{SS} of Display Clock buffer
DFB	93	O	OPF20	Fast Blanking Control signal
DY	86	O	E027	Analog Y output of DAC
DU	90	O	E027	Analog U output of DAC
DV	88	O	E027	Analog V output of DAC
DAV_{refT}	87	I	E027	Analog Top Reference for DACs
DAV_{refB}	89	I	E027	Analog Bottom Reference for DACs
DAV_{bias}	85	I	E027	Analog Voltage Reference DACs
DAV_{DDA}	83	I/O	E030	Analog V_{DD} of DACs
DAV_{SSA}	84	I/O	E009	Analog V_{SS} of DACs
DAV_{DDD}	92	I/O	E030	Digital V_{DD} of DACs
DAV_{SSD}	91	I/O	E009	Digital V_{SS} of DACs
DPH_{sync}	95	I	HPP01	Horizontal Sync Display PLL
DPV_{bias}	96	I/O	E027	Analog bias reference Display PLL
DPV_{DDA}	98	I/O	E030	Analog V_{DD} of Display PLL
DPV_{SSA}	97	I/O	E009	Analog V_{SS} of Display PLL

Pin Type explanation:

E030	V_{DD} pin, diode to V_{SS}
E009	V_{SS} pin, diode to V_{DD}
E027	Analog Input pin, Diode to V_{SS} and V_{DD}
HPP01	Digital input pin, CMOS levels, diode to V_{DD} and V_{SS}.
OPF20	Digital output pin, CMOS levels.
HPF01	Digital input pin, CMOS levels, diode to V_{SS}
IOI41	IIC pull-down output stage, CMOS input levels, diode to V_{SS}.
HUP07	Digital input pin, CMOS levels with hysteresis, pull up resistor to V_{DD}, diode to V_{DD} and V_{SS}.

5 Block Diagram

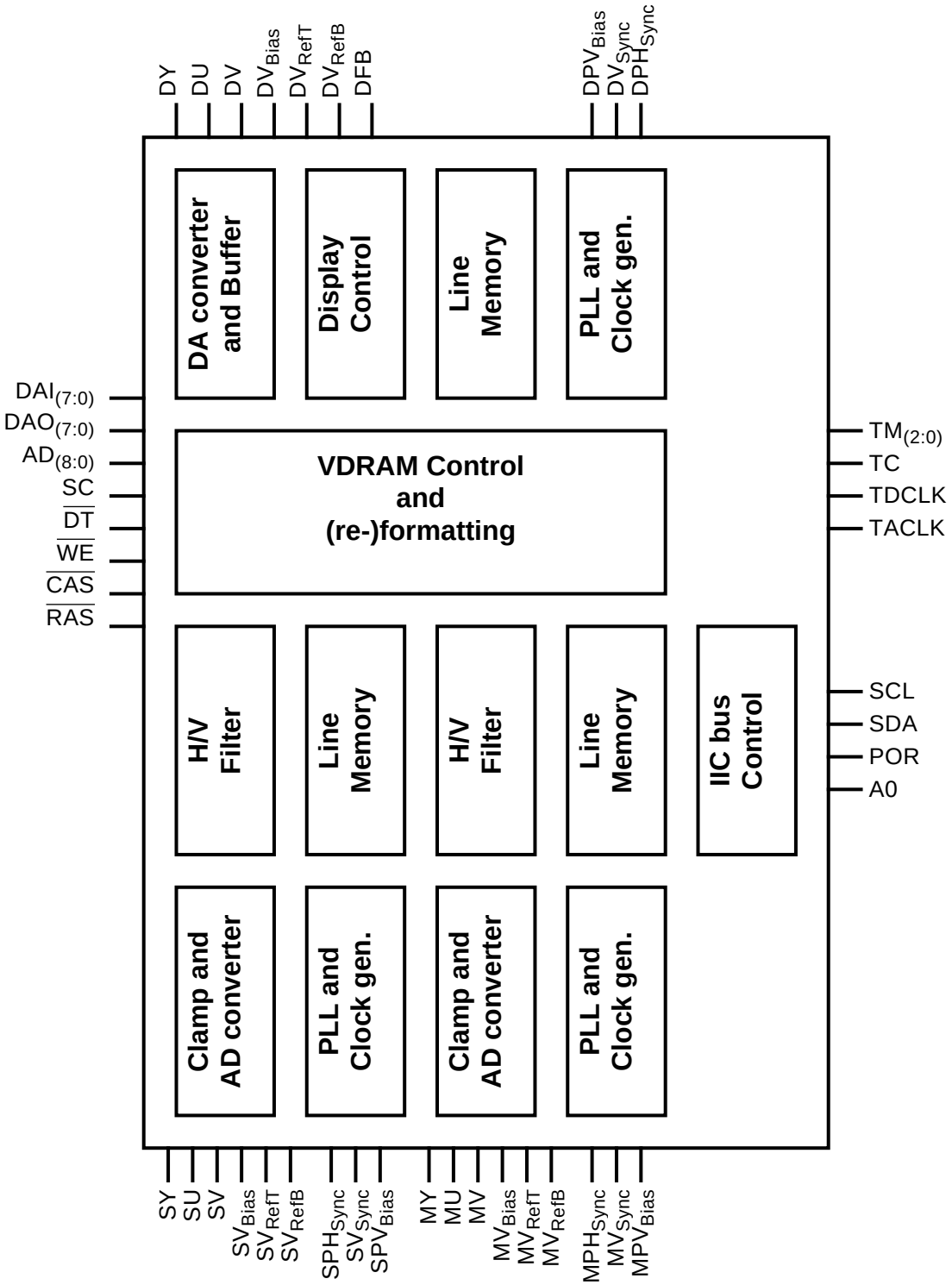

Figure 2: Block diagram of SAB9077H

Supply pins are not drawn in the diagram above.

6 Functional Description

6.1 Pixel rate

The internal Chroma format used is 4:1:1. It is expected that the bandwidth of the input signals is limited to 4.5 MHz for the Y input and 1.125 MHz for the U/V inputs.
The Y input is sampled with a 1728*HS (≈ 27.0 MHz) clock and is filtered and down sampled to the internal 864*HS (≈ 13.5 MHz) pixel rate.
The U and V inputs are multiplexed and sampled with a 432*HS clock and down sampled to the internal 216*HS (≈ 3.375 MHz) pixel rate.

6.2 Acquisition Area

Synchronisation is done via the acquisition H_{Sync} and V_{Sync} pins. With the acquisition fine positioning added to a system constant the starting point of the acquisition can be controlled.
The acquisition area is 672 pixels/line and 228 lines/field for NTSC and 276 lines/field for PAL. Both channels Main and Sub are equivalent in handling the data.

6.3 Display mode

The internal display pixel rate is 864*DPH_{Sync} which is 13.5 MHz. This pixel rate is upsampled by interpolation to 1728*DPH_{Sync} before the DAC stage.

6.4 Display Area

The display background is an area of 696 pixels for both PAL and NTSC, 238 lines for NTSC and 286 lines for PAL. This can be put ON/OFF by the BGON bit independent of the PIPON bits. This area can be moved by the Display Background fine positioning (BGhfp and BGvfp). Its color is determined by the BGCOL and BGBRT bits.
Within this area PIPs are defined dependent on the PIP mode. The PIP sizes are determined by the display reduction factors as is shown in table 1. Whether a PAL or NTSC fixed number is used is dependent on the DPAL bit.

Reduction	H1	H2	H3	H4	V1	V2	V3	V4
pixels	672	336	224	168				
NTSC-lines					228	114	76	57
PAL-lines					276	138	92	69

Table 1: PIP sizes

The display fine positioning determines the location of the PIPs with respect to the background. Sub Channel and Main Channel both have their independent PIP size and location control.
This is depicted in figure 3.

6.5 PIP modes

The two independent acquisition channels can also be controlled independently on the display side. A wide variety of modes is possible but a subset of 7 modes is fixed and can be set easily by the IIC bus. An overview of the preconditioned modes is given in table 2.
For all pip modes the Main and Sub display fine positioning must be set to obtain a display configuration.

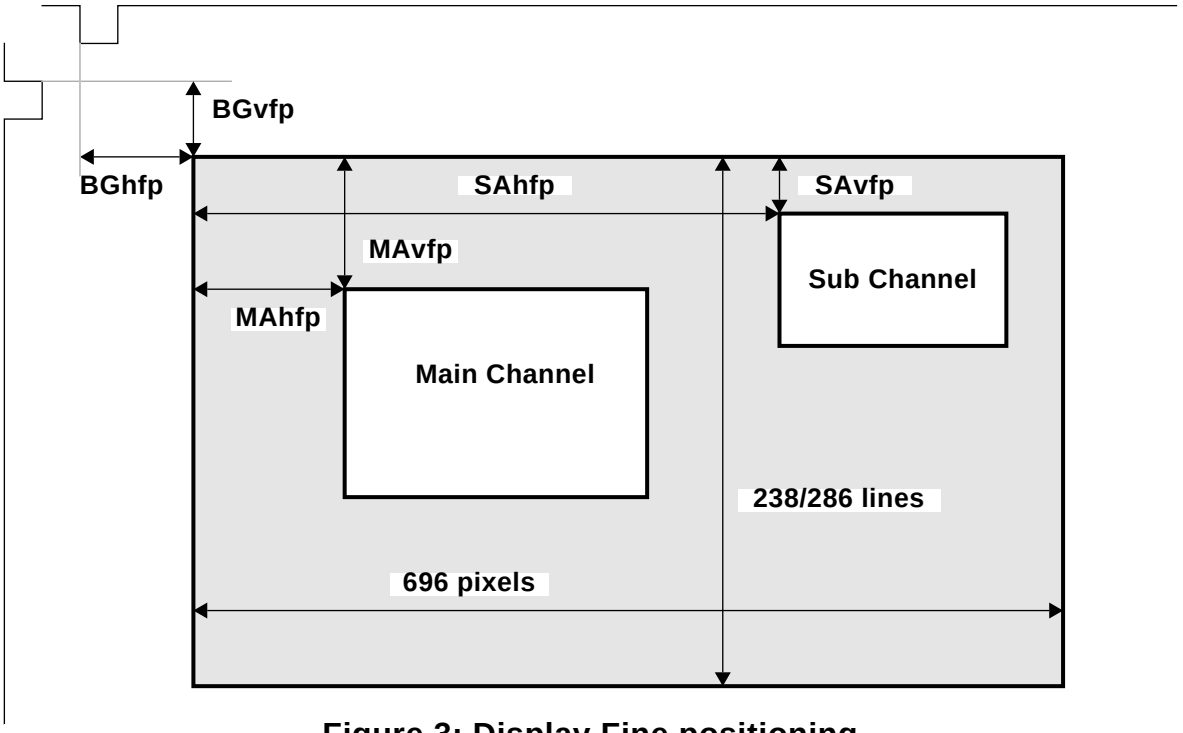

Figure 3: Display Fine positioning

6.5.1 Standard PIP modes

Table 2 shows the standard PIP modes with the settings of the reduction and position factors are displayed.

PIP Modes			Sub Channel		Main Channel		Sub Channel		Main Channel	
Name	**Figure**	**Mode**	**Hred**	**Vred**	**Hred**	**Vred**	**hfp**	**vfp**	**hfp**	**vfp**
SP	SP Small	0000	1/4	1/4	-	-	-	-	-	-
SP	SP Medium	0000	1/3	1/3	-	-	-	-	-	-
SP	SP Large	0000	1/2	1/2	-	-	-	-	-	-
SP	SP Small	0000	-	-	1/4	1/4	-	-	-	-
SP	SP Medium	0000	-	-	1/3	1/3	-	-	-	-
SP	SP Large	0000	-	-	1/2	1/2	-	-	-	-
DP	DP	0000	1/2	1/2	1/2	1/2	03h	46h	57h	46h
DP	Twin PIP	1001	1/2	1/1	1/2	1/1	03h	05h	57h	05h
MP3L	POP-Left	0010	1/4	1/4	-	-	08h	10h	-	-
MP3R	POP-Right	0010	-	-	1/4	1/4	-	-	72h	10h
MP3D	POP-Double	0010	1/4	1/4	1/4	1/4	08h	10h	72h	10h
MP7	POP-Double	0011	1/4	1/4	-	-	03h	05h	-	-
MP8	MP7	0011	1/4	1/4	1/2	1/2	03h	05h	44h	20h
MP4	Quatro	0001	1/2	1/2	1/2	1/2	03h	05h	03h	77h
MP9	MP9	0100	1/3	1/3	1/3	1/3	03h	05h	51h	3Bh
MP16	MP16	0101	1/4	1/4	1/4	1/4	03h	05h	03h	05h
MP16	MP16 Mix	0110	1/4	1/4	1/4	1/4	03h	05h	03h	77h
FFS	Full Field Still	0000	1/1	1/1	-	-	03h	05h	-	-
FFS	Full Field Still	1000	-	-	1/1	1/1	-	-	03h	05h
MAN	Manual	X111	x	x	x	x	x	x	x	x

Table 2: PIP Modes

The pictures 4 and 5 give an overview of possible combinations as they can be shown on the screen.
An example of fine positioning is given in the right four columns.

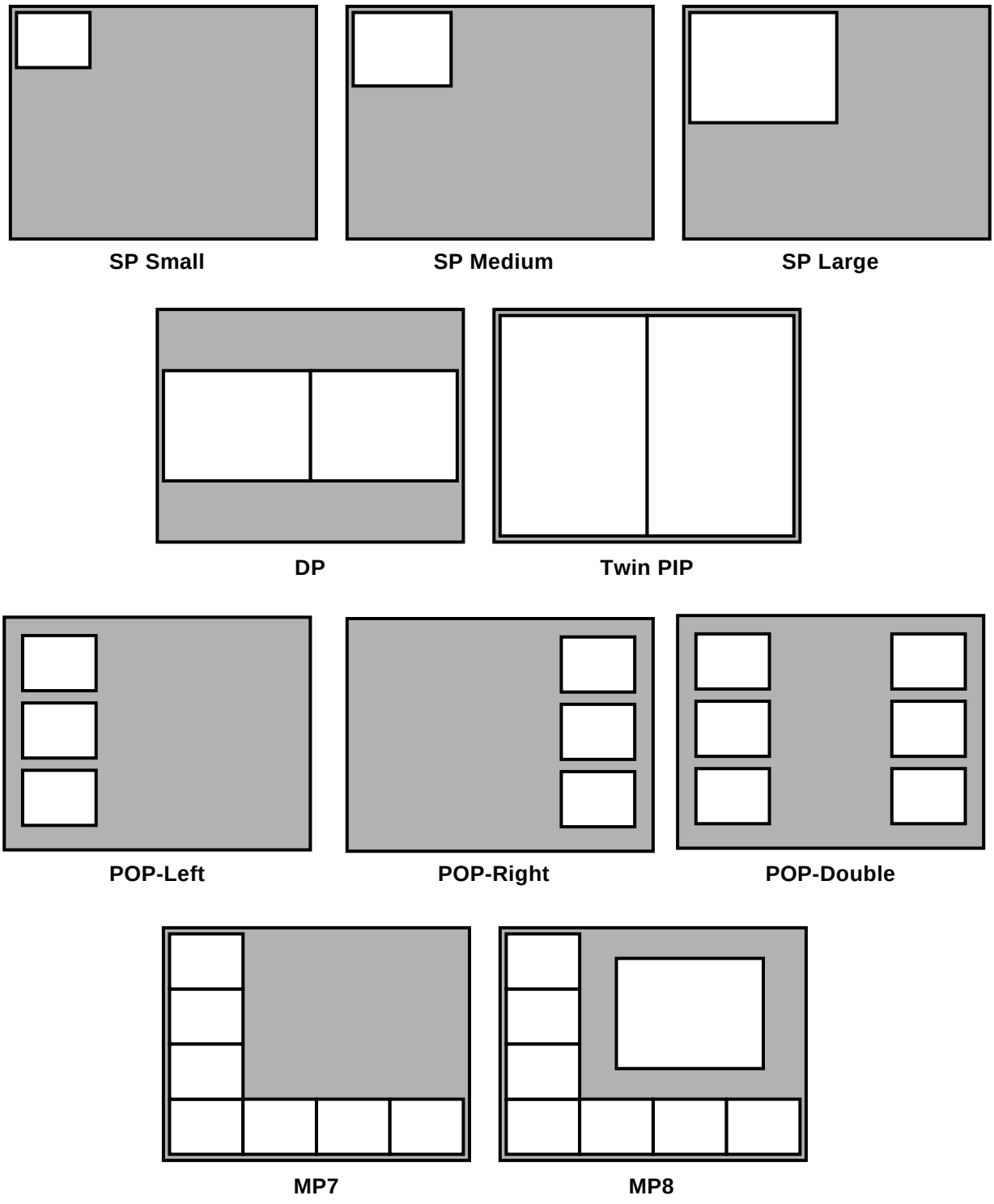

Figure 4: PIP Modes

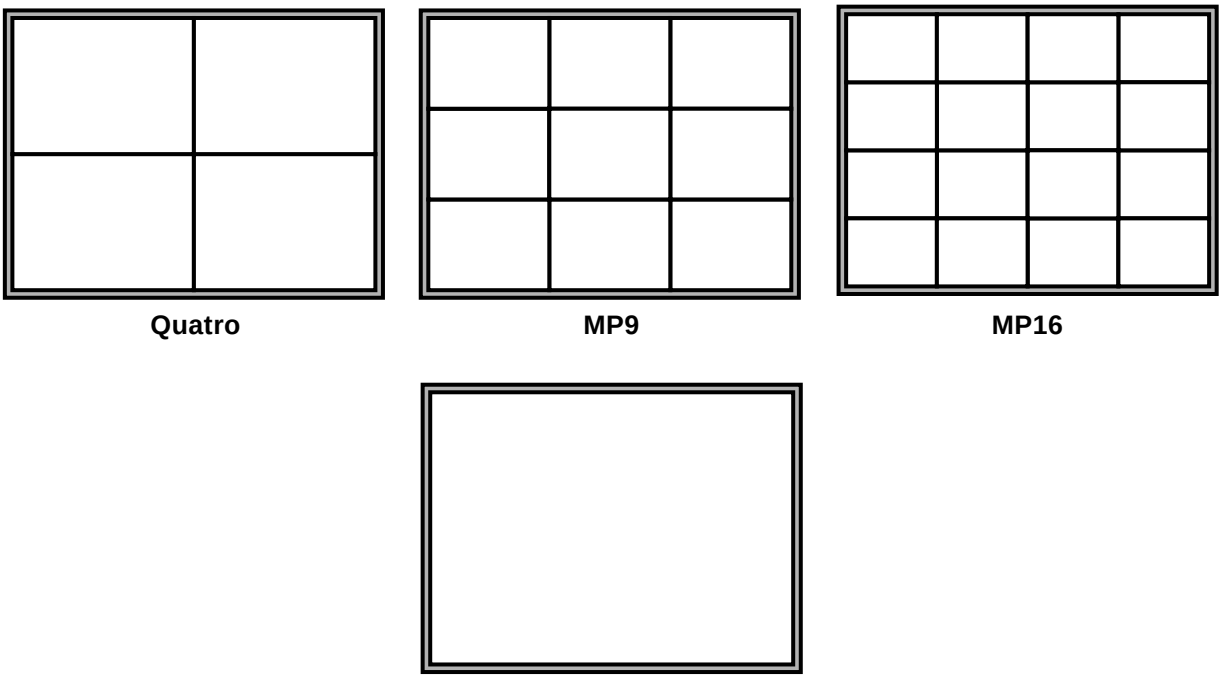

Figure 5: PIP Modes (continued)

More PiP modes can be obtained by varying the horizontal and vertical reduction factors to meet correct aspect ratios when using 16:9 screens.

In Manual Mode more pipmodes become available. Section “More settings IIC bus” on page 23 describes how to setup a pipmode.

7 Device description per functional block

The principle of the working of a Picture-in-Picture is simple. Take a picture, reduce it in size and insert it at the correct position. The first problem that arises is, that broadcasting of different channels is not synchronized. The second problem is that a reduced picture is faster displayed as it will be reduced. For instance, by reducing the picture in the vertical direction with a factor 4, x lines are displayed. For displaying the x lines 4x lines must be processed for each field.
To solve these problems, the data should be buffered and a phase difference of at least one field between the acquiring of a picture and the displaying of the created picture. The data buffer must be able to contain two reduced pictures. As long as data is required for one picture the other one can be displayed. This all holds for one single live PIP. For the buffer a DRAM, SRAM etc can be used.
Two independent live pictures makes two acquisition channels and more memory, then for one live picture necessary. There are three data streams then, two acquired data streams storing data in the memory, and one display data stream retrieving data from the memory.

The SAB9077 is organized in functional blocks (see “Block Diagram” on page 11). These different blocks are:

- PLL and clockgenerator.
- Buffer and clampcircuit.
- ADC.
- H + V Filter.
- VDRAM control and (re-)formatting.
- Data display
- Line memory
- DAC
- Output buffer ad amplifier
- IIC-control

7.1 PLL and clockgenerator

The SAB 9076 has three PLLs on-board, one for the main channel, one for the sub channel and one for the display channel.
The PLL is used to synchronize the internally used clocksignals with the incoming Horizontal synchronisation signal of a channel (H-sync). The PLL compares the reference output of the clockgenerator with the H-sync signal, produced by the decoder for that channel.
The PLL generates a clock of 27 MHz which is led into the clockbuffer.
The catching range of the PLL is 4 kHz.
Supply voltage Vbias influences the dynamic behaviour of the PLL. Higher Vbias causes the PLL to lock faster, lower Vbias causes the PLL to lock slower.
The positive edges of the H-sync signals are the driving timing points.

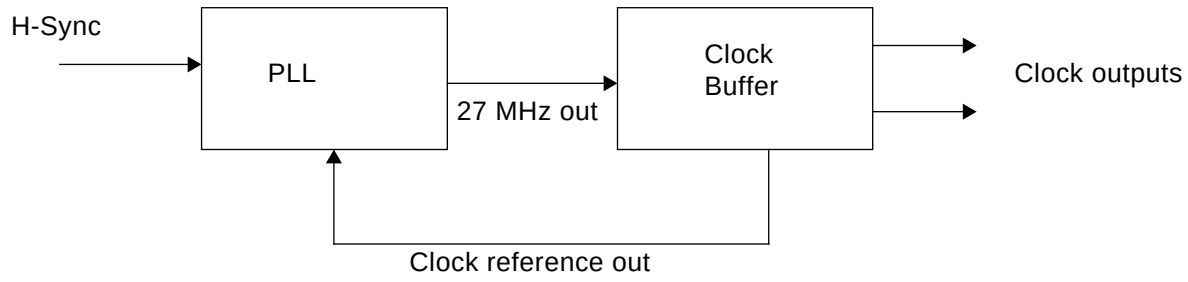

Figure 6: Block diagram of the PLL-circuit

7.2 Video-buffer and clamping circuit

The video-buffer protects the ADC for damage that could be caused by the incoming video signals. The video signals are the Y,U and V output signals of the decoder.
The overall gain of the video-buffer is 1.
The video-buffer bandwidth is 6 MHz.

The clamping circuit will clamp the luminance input signal to Vrefb, and the chrominance input signals to Vreft+Vrefb/2 + LSB/2.
The clamping starts at the active edge of the burstkey.
AC-coupling of the video input signal is done outside the PIP-IC with capacitor C, which is also used for clamping.

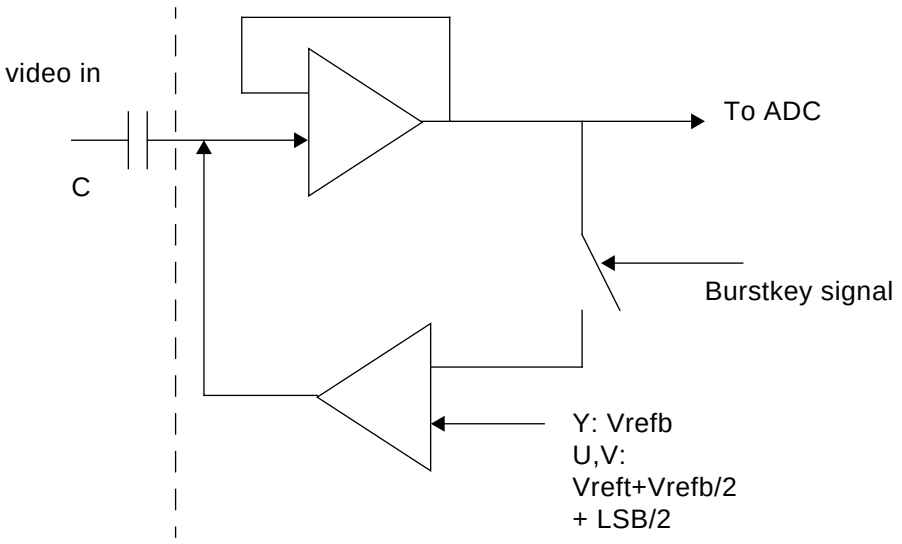

Figure 7: Video buffer and clamping circuit

7.3 Acquisition Channel ADCs

Both channels convert the analog input signals to digital signals by means of a ADCs, one for each channel. The input levels of the ADCs of each channel are equal and can set by the AV_{refT} and AV_{refB} pins. The reference levels V_{refT} and V_{refB} are made internally by a resistor division of the VDD. They can be calculated with the formulas $V_{reft} = AV_{DD}$ x (2.1/5.0) Volt and $V_{refB} = AV_{DD}$ X (0.4/5.0) Volt
External capacitors are needed to filter AC components on the reference levels. The resolution of the ADCs is 8 bit (DNL is 7 bit, INL is 6 bit) and the sampling is done at the system frequency of 27 MHz for the Y-input. The U/V inputs are multiplexed and sampled at 13.5 MHz.
The analog input signals are amplified to make maximum use of the dynamic range of the ADCs.
A bias voltage V_{bias} is used for decoupling AC components on internal references. The inputs should be AC-coupled and an internal clamp circuit will clamp the input to AV_{refB} for the luminance channels and to (AV_{refT} - AV_{refB})/2+LSB/2 for the chrominance channels. The clamping starts at the active edge of the burst key.

7.4 H + V Filters

The horizontal and vertical filters take care that the data that will be stored in the VDRAM have the right dimensions. This means that the horizontal and vertical size are made into the size needed for the chosen PIP mode.
The horizontal filters will compress the picture to the horizontal size of the chosen PIP mode.
The vertical filters will compress the picture to the vertical size of the chosen PIP mode.

7.5 VDRAM control and (re-)formatting

7.5.1 Memory interface

The SAB9077 consists of three parts, two acquisition channels and a display channel. The acquisition channels filters and decimates the incoming pictures both horizontally and vertically. This depends on the PIP-mode that is selected. The result of this process will be formatted from an internal into a 8 bit format which fits in the external VDRAM. The display channel fetches the data from the external VDRAM and reformats it into an internal format again.
The three parts have their own clockdomain and their own VDRAM control. Since only one part at the time may have control over the VDRAM a controller is present to regulate the priorities and the switching over from one VDRAM-controller to another. Furthermore it has to activate a refresh controller, if the acquisition and the display channels are inactive. This controller is the VDRAM-arbiter.

7.5.2 VDRAM arbiter

The VDRAM arbiter has four tasks:

1. Give the control over the VDRAM to the VDRAM controller of which the request has the highest priority.

2. Activate the refresh controller, if none of the others requests the control.

3. Switch smoothly from one controller to another, because of the edge sensitivity of the VDRAM.

4. Activate the load-address calculator and generate a load pulse for the first line of a channel.

The first time in a field, a controller makes a request, a load address must be calculated. The VDRAM controller signals this to the VDRAM arbiter by a firestone signal. The VDRAM arbiter will activate a central address calculator the dependent of channel type, channel number, system type, horizontal reduction, vertical reduction and internal format use, will determine a loadaddress. This loadaddress connects via a bus to all three address counters. The VDRAM arbiter selects one of them by a load pulse. The load pulse also acts as a reset for the firstline signal. This prevents unnecessary reloading/recalculation. By centralising the generation of the loadaddress, it will be assured that the loadaddress for reading and writing is always the same.

7.5.3 external VDRAM

A VDRAM is a normal DRAM which has been modified to ease the handling of video-data. The base of the concept is that video-data most of the time will be handled in blocks in which the pixels have successive numbering. The modification of a normal DRAM is merely adding a large shiftregister that can be accessed almost independently. Furthermore, a lot of block and row oriented modes are present. Only three of them are used by the SAB9077. These modes are:

1. Page write mode.
2. Read transfer mode
3. CAS before RAS refresh with automatic row addressing.

Most modes work with a Row Access Strobe (RAS), which validates the address, and a Column Access Strobe (CAS), which validates the address as a column address. The VDRAM is sensitive to falling edges of the control signals. With the exception of the shiftclockregister. The shiftclockregister is bidirectional. Data can be shifted out (Read) or shifted in (Write). The type of it will be set by the previous transfer cycle.

For the external memory one VDRAMs of type NEC D482 234 LE-70 is foreseen. It has a storage capacity of 262144 words of 8 bit each.
It is also possible to use two 1MB VDRAM of 262144 words of 4 bit.

7.6 Data display

The Data display part takes care of the controls at the display part of the SAB9077.
The data display part controls:
1. Border (size, color, brightness etc.).
2. Place on the television screen.
3. Line memory control.
4. Data stream to the DACs.
5. Synchronisation.

7.7 Line memory

In the SAB9077 there are four line memories on board. These memories are used to store the data of one line. At the right time, determined by the synchronisation, this memory will be read.
The line memories are used to organize the timings in the SAB9077.

The display part uses two line memories. The first line memory is used to write data in, when the second line memory is read. When the second line memory is written, the first line memory is read.

7.8 Output DACs

The digital processed signals are converted to analog signals by means of three 8 bit DACs. The output voltages of these DACs are default set by the DAV_{refT} pin for the top level and DAV_{refB} pin for the bottom level. Default values are 1.5 V.

7.9 Output buffer and amplifier

Default signal levels for the output signals DY, DU and DV are 1.5 Vpp. This means that the overall gain of the SAB9077 is 1.

The output signals DY, DU and DV are made lowohmic by means of the output buffers between the DACs and the output pins.

The output load resistors should be 220 to get the overall gain of 1.

The output buffer has a unit voltage gain and a output resistance of 25 Ohm. So when the load resistance Rill = 220 Ohm, the gain is 220/245.
A unit gain is therefore achieved when the DAC input range equals 245/220 times the ADC input range.
DAC (Vreft - Vrefb) = 245/220 * 1.7 = 1.9 V. So Vreft - Vrefb must be 1.9 V, the default values are Vrefb = 0.4 V and Vreft = 2.3 V
For the ADC input range see section “Analog decoder settings” on page 41

7.10 IIC bus description

The IIC bus provides bi-directional 2-line communication between different ICs. The SDA line is the serial data line and the SCL serves as serial clock line. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.
The SAB9077H has the IIC addresses 2C and 2E, switchable by the pin A0. Valid sub addresses are 00H to 18H and 20H to 32H. IIC bus control is according to the IIC bus protocol:
First a start sequence must be put on the IIC bus, then the IIC address of the circuit must be send, then a sub address. After this sequence the data of the sub addresses must be send. An auto increment function gives the option to send data of the incremented sub addresses until a stop sequence is send.
Table 3 gives an overview of the IIC bus addresses.

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Sub Address	Data Bytes							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H	MPIPON	SPIPON	MFreeze	SFreeze	MCopy	$PiPMode_{(2:0)}$		
01H	-	-	M1FLD	S1FLD	NiPCoff	DNonInt	MNonInt	SNonint
02H	DFilt	FILLOFF	SMART6	SKIP6	$Yth_{(3:0)}$			
03H	$BGhfp_{(3:0)}$				$BGvfp_{(3:0)}$			
04H	$SDhfp_{(7:0)}$							
05H	$SDvfp_{(7:0)}$							
06H	$MDhfp_{(7:0)}$							
07H	$MDvfp_{(7:0)}$							
08H	$MDRedH_{(1:0)}$		$MDRedV_{(1:0)}$		$SDRedH_{(1:0)}$		$SDRedV_{(1:0)}$	
09H	$MARedH_{(1:0)}$		$MARedV_{(1:0)}$		$SARedH_{(1:0)}$		$SARedV_{(1:0)}$	
0AH	$MAhfp_{(3:0)}$				$SAhfp_{(3:0)}$			
0BH	$SAvfp_{(7:0)}$							
0CH	$MAvfp_{(7:0)}$							
0DH	$MLsel_{(3:0)}$				$SLsel_{(3:0)}$			
0EH	$MBsel_{(3:0)}$				$SBsel_{(3:0)}$			
0FH	$Bhsize_{(3:0)}$				$Bvsize_{(3:0)}$			
10H	-	SBON	$SBbrt_{(1:0)}$		-	$SBcol_{(2:0)}$		
11H	-	SBSON	$SBSbrt_{(1:0)}$		-	$SBScol2_{(2:0)}$		
12H	-	MBON	$MBbrt_{(1:0)}$		-	$MBcol_{(2:0)}$		
13H	-	MBSON	$MBSbrt_{(1:0)}$		-	$MBScol_{(2:0)}$		
14H	-	BGON	$BGbrt_{(1:0)}$		-	$BGcol_{(2:0)}$		
15H	-	-	-	SVfilt	SUVPol	SVSPol	SH_{sync}	SFPol
16H	-	-	-	MVfilt	MUVPol	MVSPol	MH_{sync}	MFPol
17H		$FBdel_{(2:0)}$			DUVPol	DVSPol	DH_{sync}	DFPol
18H	$PedestV_{(3:0)}$				$PedestU_{(3:0)}$			

Table 3: Overview of IIC bus sub addresses

The Data Bits which are not used should be set to zero.

More settings IIC bus

In Manual mode more PIP modes become available. An overview of these IIC bus registers is given in table 3.

Sub Address	Data Bytes							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20H	PRIO	DPal	MPal	SPal	$MVRpN_{(1:0)}$		$SVRpN_{(1:0)}$	
21H	$MHRpO3_{(1:0)}$		$MHRpO2_{(1:0)}$		$MHRpO1_{(1:0)}$		$MHRpO0_{(1:0)}$	
22H	$MHRpN3_{(1:0)}$		$MHRpN2_{(1:0)}$		$MHRpN1_{(1:0)}$		$MHRpN0_{(1:0)}$	
23H	$MHPic_{(7:0)}$							
24H	$MVPic_{(7:0)}$							
25H	$MHDis0_{(7:0)}$							
26H	$MHDis1_{(7:0)}$							
27H	$MHDis2_{(7:0)}$							
28H	$MHDis3_{(7:0)}$							
29H	$MVDis_{(7:0)}$							
2AH	$SHRpO3_{(1:0)}$		$SHRpO2_{(1:0)}$		$SHRpO1_{(1:0)}$		$SHRpO0_{(1:0)}$	
2BH	$SHRpN3_{(1:0)}$		$SHRpN2_{(1:0)}$		$SHRpN1_{(1:0)}$		$SHRpN0_{(1:0)}$	
2CH	$SHPic_{(7:0)}$							
2DH	$SVPic_{(7:0)}$							
2EH	$SHDis0_{(7:0)}$							
2FH	$SHDis1_{(7:0)}$							
30H	$SHDis2_{(7:0)}$							
31H	$SHDis3_{(7:0)}$							
32H	$SVDis_{(7:0)}$							

Table 4: Overview of IIC bus sub addresses (continued)

8 Application information

8.1 Standard application for 1 FH mode

The application diagram for 1 FH mode in a standard configuration is shown in figure 8. Two input signals Main CVBS and Sub CVBS of different sources are processed by the SAB9077H and inserted by the YUV/ RGB switch. The synchronisation of the display PLL is derived from the deflection circuit. The main signals are also led to the deflection circuit and the YUV/RGB switch where the SAB9077H signals can be inserted. The signals for deflection can also be taken from the Main Channel or Sub Channel decoder.

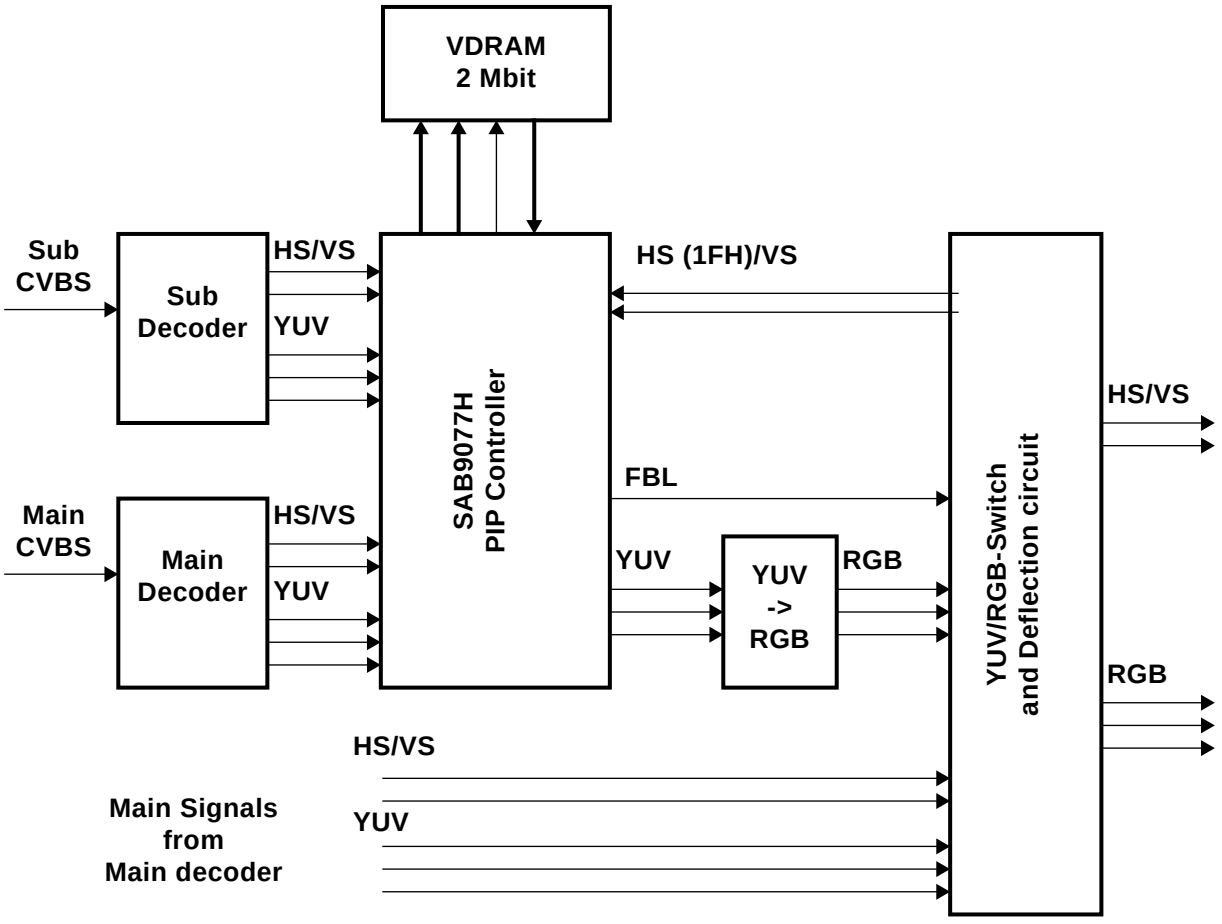

Figure 8: Application diagram 1 FH mode. Main-channel processed as PIP sub channel + one independent sub-channel.

8.2 Non standard application for the 1FH mode

The application diagram for 1 FH mode in a non- standard configuration is shown in figure 8 Two input signals Main CVBS and Sub CVBS of different sources are processed by the SAB9077H and inserted by the YUV/ RGB switch. The synchronisation of the display PLL is derived from the Display- circuit. The Display-signals are also led to the deflection circuit and the YUV/RGB switch where the SAB9077H signals can be inserted.

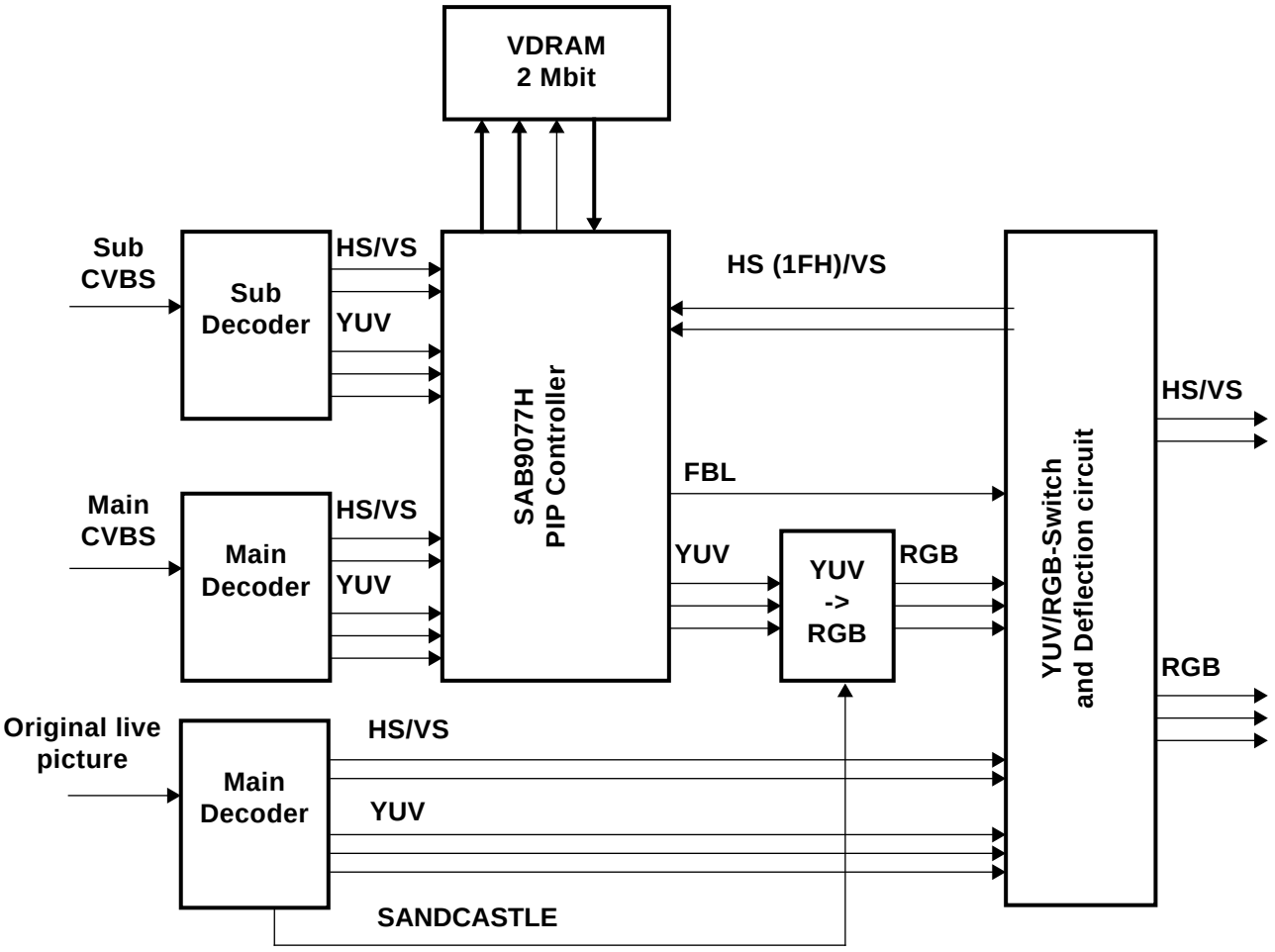

Figure 9: Application diagram 1 FH mode Original live picture as background + two independent PIP-channels.

8.3 VCR application for the 1 FH mode

The application diagram for 1 FH mode in a VCR configuration is shown in figure 8. Two input signals Main CVBS and Sub CVBS of different video sources are processed by the SAB9077H and inserted by the YUV/ RGB switch. The synchronisation of the display PLL is derived from the Main circuit. The main signals also takes care of the synchronisation of the two video-sources inside the VCR.
The video sources can be two video-signals from one tape or two video signals from two tapes played on the same VCR.

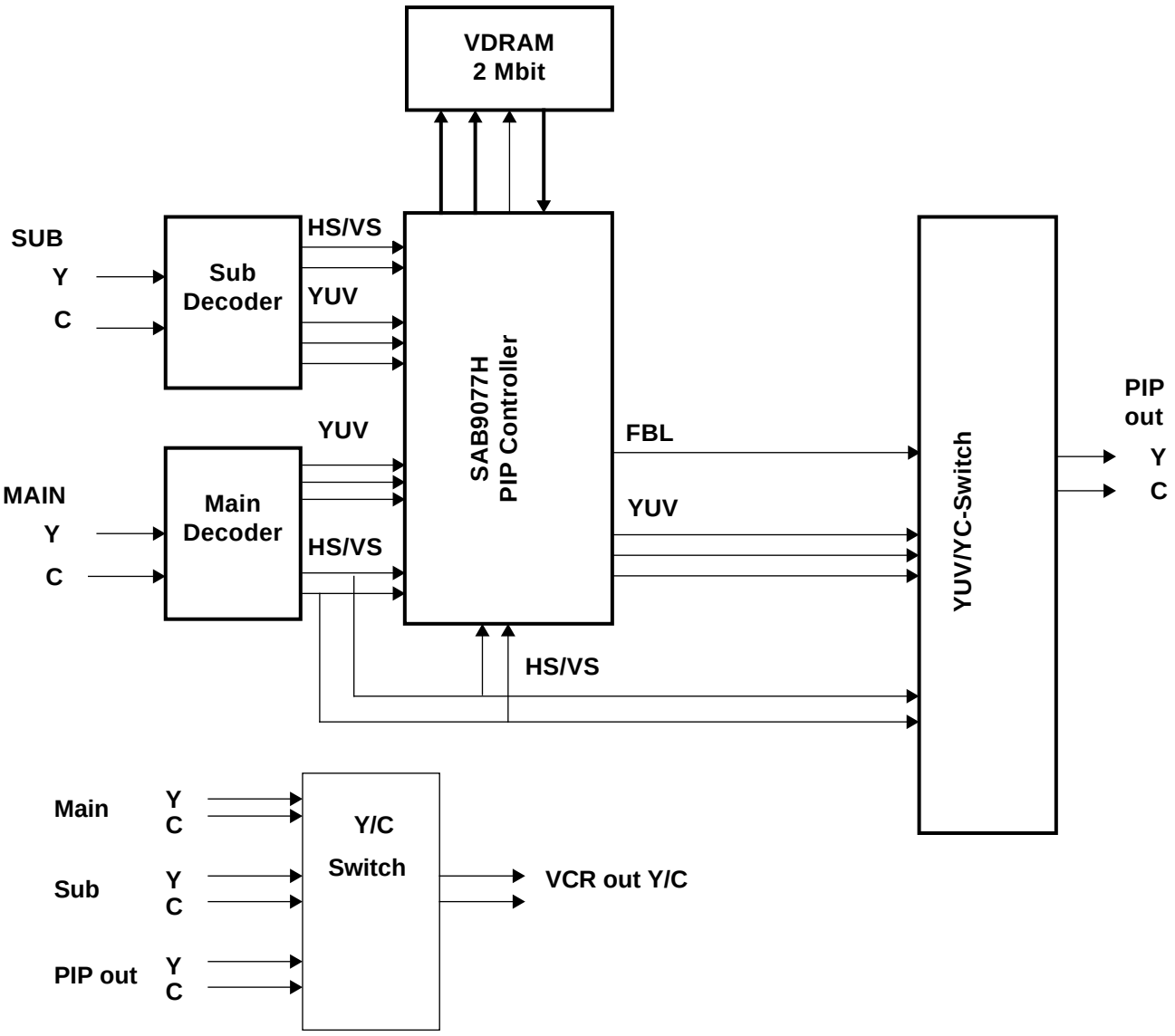

Figure 10: VCR-Application diagram 1 FH mode

9 Functionality of the PIP controller SAB9077

The content of the 44 register IIC-bus interface defines the functionality of the PIP controller SAB 9076. The IIC bus interface behaves like a slave receiver device.

9.1 PIP modes

9.1.1 Enabling the PIP function

After power-up is activated the SAB9077 starts up in the standard mode. In the standard mode all IIC settings are set to 0. So all registers of the IIC settings contain 00 H(exadecimal).
Setting the bit MPIPON (or SPIPON) will activate the Main (Sub) PIP and the Fast Blanking signal (DFB signal). Now the picture in picture signals are merged into the television signal with the help of an external video switch.

9.1.2 Standard PIP modes

The controller SAB9077 provides several modes to the TV system. The standard PIP modes can be selected by the mode bits PiPMODE(3, 2, 1, 0) and the reduction bits MDRedH and MDRedV for the main channel, SDRedh and SDRedV for the sub channel.

All these bits should be set properly to get a PIP on the screen.
Which PIP will be displayed on the television screen depends on the setting of the bits MPIPON and SPIPON.

The reduction factors Hred and Vred for the main- and sub channel, displayed in table Table 2, “PIP Modes,” on page 14, are the same for display and acquisition.

The only difference between the PIP modes MP7 and MP8 is, that in the MP8 mode the main channel PIP is switched ON.

PIP Modes			Sub Channel		Main Channel		Sub Channel		Main Channel	
Name	**Figure**	**Mode**	**Hred**	**Vred**	**Hred**	**Vred**	**hfp**	**vfp**	**hfp**	**vfp**
SP	SP Small	0000	1/4	1/4	1/4	1/4	-	-	-	-
SP	SP Medium	0000	1/3	1/3	1/3	1/3	-	-	-	-
SP	SP Large	0000	1/2	1/2	1/2	1/2	-	-	-	-
DP	DP	0000	1/2	1/2	1/2	1/2	03h	46h	57h	46h
DP	Twin PIP	1001	1/2	1/1	1/2	1/1	03h	05h	57h	05h
MP3D	POP-Double	0010	1/4	1/4	1/4	1/4	08h	10h	72h	10h
MP7	POP-Double	0011	1/4	1/4	-	-	03h	05h	-	-
MP8	MP7	0011	1/4	1/4	1/2	1/2	03h	05h	44h	20h
MP4	Quatro	0001	1/2	1/2	1/2	1/2	03h	05h	03h	77h
MP9	MP9	0100	1/3	1/3	1/3	1/3	03h	05h	51h	3Bh
MP16	MP16	0101	1/4	1/4	1/4	1/4	03h	05h	03h	05h
MP16	MP16 Mix	0110	1/4	1/4	1/4	1/4	03h	05h	03h	77h
FFS	FullFieldStill	0000			1/1	1/1			03h	05h
FFL	FullFieldLive	1000	-	-	1/1	1/1	-	-	03h	05h
MAN	Manual	X111	x	x	x	x	x	x	x	x

Table 5: PIP Modes

9.1.3 Mode bits PiPMode (0, 1, 2, 3)

PIP Modes		
Name	**Figure**	**Mode**
SP	SP Small	0000
SP	SP Medium	0000
SP	SP Large	0000
DP	DP	0000
DP	Twin PIP	1001
MP3D	POP-Double	0010
MP7	POP-Double	0011
MP8	MP7	0011
MP4	Quatro	0001
MP9	MP9	0100
MP16	MP16	0101
MP16	MP16 Mix	0110
FFS	FullFieldStill	0000
FFL	FullFieldLive	1000
MAN	Manual	X111

Table 6: Standard PIP Modes

The standard in the SAB9077 integrated PIP modes are displayed in table Table 2, “PIP Modes,” on page 14. With the bits PiPMode (0, 1, 2, 3) the PIP mode can be selected. The settings for the bits PiPMode and the corresponding PIP mode are displayed in Table 2, “PIP Modes,” on page 14
In the manual mode more PIP modes become available. For more information on the manual mode see section “Manual mode” on page 52.

9.1.4 Reduction factor settings

The SAB9077 provides several bits to change the reduction factors of the main- and sub channel PIP.

There are two kinds of reduction factors
1. Display reduction factors
2. Acquisition reduction factors

Normally the horizontal display- and acquisition reduction factors should be the same.
The vertical display reduction factor should be equal or smaller than the vertical acquisition reduction factor.
When the horizontal reduction factor is set to 1/1, the vertical reduction factor MUST be set to 1/1

9.1.4.1 Main/Sub channel display reduction factors

The display reduction factors determine the size of the PIP on the television screen.
Adjustment of the display reduction factor of the main- and sub channel PIP can be done with the bits MDRedH, SDRedH, MDRedV and SDRedV.

XDRedH	Horizontal display reduction factor in 4 steps. The steps are 1/1, 1/2, 1/3, 1/4.
XDRedV	Vertical display reduction factor in 4 steps. The steps are 1/1, 1/2, 1/3, 1/4.

Picture size	XDRedX	
1/4	0	0
1/1	0	1
1/2	1	0
1/3	1	1

Table 7: Settings of the display reduction factors and obtained picture size.

9.1.4.2 Main/sub channel acquisition reduction factors

The acquisition reduction factors determine the size of the picture inside the PIP on the television screen. Adjustment of the acquisition reduction factors of the main- and sub channel can be done with the bits MARedH, SARedH, MARedV and SARedV.

XARedH	Horizontal acquisition reduction factor in 4 steps. The steps are 1/1, 1/2, 1/3, 1/4.
XARedV	Vertical acquisition reduction factor in 4 steps. The steps are 1/1, 1/2, 1/3, 1/4.

Picture size	XARedX	
1/4	0	0
1/1	0	1
1/2	1	0
1/3	1	1

Table 8: Settings of acquisition the reduction factors and obtained picture size.

9.1.5 Copy mode

The copy mode is a special mode, needed for the Twin PIP mode.

In the copy mode data of the main channel PIP are not send to the VDRAM. These data are directly routed to the display buffer, after passing the H and V reduction part of the SAB9077.
For this reason the settings of the bits DPAL and MPAL must be the same in the copy mode. If MPAL is set to “1” (PAL), DPAL must also be set to “1” (PAL).

Working this way saves a lot of memory space. If the data of the main channel PIP would be send to the VDRAM, the memory would be too small to make a Twin PIP in 8 bit resolution.

When the copy mode is ON, the vertical acquisition position of the main channel can not be adjusted.

9.1.6 Freeze function

The main- and sub channel can be frozen separately by setting the bits MFREEZE and SFREEZE. The writing to the VDRAM is stopped.

XFREEZE = 0	Picture in the PIP is live
XFREEZE = 1	Picture in the PIP is frozen

9.2 Data transfer settings

The data transfer mode determines the way in which order data is transferred to the external VDRAM.
The internal datapath has an 8 bit resolution and 4:1:1 data format. The communication to the external VDRAM takes place at 864 * H-sync. For display as well as for acquisition.
Appr. 800 8 bit words can be fetched from the external VDRAM in one display line which is not enough to display one complete display line with true 8 bit resolution. Two ways of reducing data are available. One is simply skipping the 8 bit to 6 bit (SKIP6 IIC bit) and the other one is a small form of data reduction to come from 8 bit to 6 bit (SMART6 IIC bit). If both bits are ‘0’ the device is in true 8 bit resolution mode.
The data transfer mode can be selected with the bits SMART6 and SKIP6. The SAB9077 is in the 8-bit mode after start-up.

Selection of the data transfer modes with the bits SKIP6 and SMART6

D.T.MODE	SMART6	SKIP6
8 bit	0	0
smart 6	1	0
skip 6	0	1

Table 9: Settings of SMART6 and SKIP6 and the obtained data transfer mode

For the Twin PIP mode the main channel is not placed in the VDRAM but in an internal buffer, see 9.1.5 “Copy mode” on page 29.

9.3 Border settings

The SAB9077 provides several bits to generate a border around the displayed PIPs.
Features of this generated border are:

1. The border can be switched ON or OFF.
2. The border color and brightness can be adjusted.
3. The border can be changed in size, that means height and width can be adjusted.

One PIP for the main- and the sub channel can be selected and accentuated with a different color, with the Main (Sub) border select. E.g. to show which PIP displays the live picture, or to point out which picture in the Multi PIP mode should become the live picture on the television screen. Features border select:

1. The border select can be switched ON or OFF
2. The color of the border select can be adjusted.
3. The selected PIP, around which the border select is placed can be changed, to indicate a certain PIP.

9.3.1 Border ON/OFF

The borders around the Main- or Sub PIPs can be switched ON or OFF with the bits MBON and SBON.

XBON = 0	Border is set to off.
XBON = 1	Border is set to on.

The border will start at the same point where the displaying of the PIPs starts.
In single PIP modes the start-point of the borders is determined by the horizontal and vertical fine positioning (bits XDhfp and XDvfp).
In Multi PIP modes the start-point of the border around PIP 0 is determined by the horizontal and vertical fine positioning (bits XDhfp and XDvfp). The borders around the other PIPs will be calculated from the start-point of the PIP.

When the size of the borders is changed picture data of lines and pixels will be changed into border data towards the centre. How much lines and pixels are changed depends on the setting of the border-size.

9.3.2 Border color and brightness

The brightness and color of the main- and sub channel border is adjustable with the bits MBBRT, MBCOL, SBBRT and SBCOL.

Brightness bit XBBRT: 4 steps 30%, 50%, 70%, 100%.
color bit XBCOL: 8 steps black, blue, red, magenta, green, cyan, yellow, white.

Totally there are 8 colors in 4 degrees of brightness each, this means totally 32 colors.
By setting the DUVpol to 1 another 32 colors come available, but the color of the background is then also restricted to this 32 colors, see “Polarity of the border and background colors” on page 34

Table 10 indicates how IIC register settings control the color and brightness. All color registers are similar, they contain one On/Off bit, two brightness bits and three color type bits.

Color Type		Brightness level			
Color	**Value**	4-H	5-H	6-H	7-H
Black	-0H	0%	10%	30%	50%
Blue	-1H	30%	50%	70%	100%
Red	-2H	30%	50%	70%	100%
Magenta	-3H	30%	50%	70%	100%
Green	-4H	30%	50%	70%	100%
Cyan	-5H	30%	50%	70%	100%
Yellow	-6H	30%	50%	70%	100%
White	-7H	60%	70%	80%	100%

Table 10: Color Types and Brightness levels

Black and white do not contain any chrominance information. This means that black and white only contain luminance information and are no real colors. That means that a 30% white and a 30% black will show the same gray picture.
Now the ranges of black and white can be fit together to make one gray scale. All the values in this gray-scale are measured as function of the 100% white level. The gray scale is shown in figure 11.

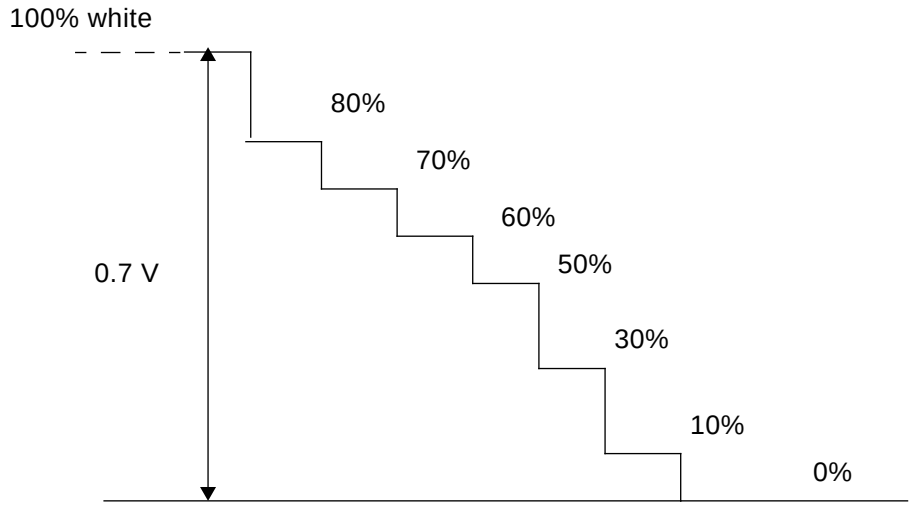

Figure 11: Gray scale of the values of black and white brightness

9.3.3 border-size

The register 0FH controls the border-size. This implies that border-sizes of the main- and sub channel are changed at the same time, which means that all borders have the same size.

The minimum horizontal border-size is 2 pixels,.
The minimum vertical border-size is 1 line.

The vertical border-size is multiplied by the FH mode number before it is displayed on the screen. This means in the 2 FH mode the border-size is 2* the border-size in 1FH mode.

Horizontal border-size Bhsize : 16 steps of 2 pixels. So maximum horizontal border-size is 32 pixels.
Vertical border-size Bvsize : 16 steps of 1 line. So maximum vertical border-size is 16 lines.

When the size of the border becomes bigger, picture data of lines and pixels will be changed into bordered towards the centre. How much lines and pixels are changed depends on the setting of the border-size.

9.3.4 Border select

One PIP of the Main channel as well as one PIP of the Sub channel can be given a different color. For example to indicate which PIP shows the live picture at the moment. The Main border select is controlled with MBSON (For Sub channel: SBSON).

SBSON = 0 Border select is OFF.
SBSON = 1 Border select is ON.

The PIP around which the border select is placed, can be selected with the $SBsel_{(0:3)}$ bits. To enable selection, SBSON must be '1'.

SBsel	Border selected
0 H	0
1H	1
2 H	2
3 H	3
4 H	4
5 H	5
6 H	6
7 H	7
8 H	8
9 H	9
A H	10
B H	11
C H	12
D H	13
E H	14
F H	15

Table 11: Border selection with SBsel

The color of the border select is determined by the bits MBSbrt and MBScol, in he same way as explained for the border color and brightness (see "Border Colour and brightness" on page 36).

Television channel selection in a multi PIP mode can be made with the border select.

1. On the television screen choose the television channel that should become the live picture with the border select.
2. The uP that controls the SAB9077, can select the right channel now, with the latest data send to the XLsel register 0D H.

9.3.5 Border priority

To determine which color is visible in case two or more colors will be displayed on the same position the next priority scheme is followed:

1. Sub Select Color (SBS)
2. Sub Border Color (SB)
3. Main Select Color (MBS)
4. Main Border Color (MB)
5. Background Color (BG)

Sub Select Color has priority over Sub Border Color because otherwise the selected border will have the same color as the other borders.
The priority of Sub over Main is determined by the priority bit, see section “Priority bit” on page 37.

9.3.6 Polarity of the border and background colors

The U,V polarity of the border and background colors can be inverted with the bit DUVpol.

DUVpol = 0	U, V polarity.
DUVpo = 1	-U, -V polarity.

9.4 Background settings

The SAB9077 provides several bits to generate a background behind the PIPs. The background has a fixed size 696 pixels and 238 lines, if there is no other PIP or framing information.
Features of the background:

1. Background can be switched ON or OFF.
2. Background positioning can be adjusted
3. Background color can be adjusted
4. Background transparency can be adjusted

9.4.1 Background ON/OFF

The background can be switched ON or OFF with the bit BGON.

BGON = 0 Background switched OFF.
BGON = 1 Background switched ON.

9.4.2 Background color and brightness

The brightness and color of the background is adjustable with the bit settings BGbrt and BGcol.
Brightness bits MBBRT : 4 steps 30%, 50%, 70%, 100%.
Color bits MBCOL : 8 steps black, blue, red, magenta, green, cyan, yellow, white.

Totally there are 8 colors in 4 degrees of brightness each, this means totally 32 colors.
By setting the DUVpol to 1 another 32 colors come available, but the color of the borders are then also restricted to this 32 colors, see “Polarity of the border and background colors” on page 34.

Table 10 indicates how IIC register settings control the color and brightness. All color registers are similar, they contain one On/Off bit, two brightness bits and three color type bits.

Color Type		Brightness level			
Color	**Value**	4-H	5-H	6-H	7-H
Black	-0H	0%	10%	30%	50%
Blue	-1H	30%	50%	70%	100%
Red	-2H	30%	50%	70%	100%
Magenta	-3H	30%	50%	70%	100%
Green	-4H	30%	50%	70%	100%
Cyan	-5H	30%	50%	70%	100%
Yellow	-6H	30%	50%	70%	100%
White	-7H	60%	70%	80%	100%

Table 12: Color Types and Brightness levels

9.4.3 Background positioning

The position of the background can be adjusted within certain limits. The bits $BGhfp_{(3:0)}$ and $BGhvp_{(3:0)}$ control the adjustment of the background position.
Horizontal position $BGhfp_{(3:0)}$: 16 steps of 4 pixels. So the maximum adjustment range is 64 pixels.
Vertical position $BGvfp_{(3:0)}$: 16 steps 0f 2lines/field. So the maximum adjustment range is 36 lines/field.

This means the background can be shifted 64 pixels horizontally and 32 lines/field vertically.

9.4.4 Luminance Threshold Yth

Luminance threshold means that the original live picture (partially) can be seen through the PIPs.

The level of transparency is set with $Yth_{(3:0)}$.
With $Yth_{(3:0)}$ the slicing level is adjusted. All luminance levels beneath the slicing level will be cut out and filled with the original live picture.

Yth = 0 H	No transparency, so nothing of the original live picture can be seen through the PIPs.
Yth = F H	Maximum transparency, the original live picture can be seen through the PIPs

If $Yth_{(3:0)}$ becomes maximum, the fast blank signal is switched off and the original live picture will be visible.

If borders are used around the PIPs, the borders will remain visible, even when Yth is set to maximum. The fast blank signal is not switched off.
If a back ground is used, the original live picture can be seen through the PIPs, not through the background. The fast blank signal is not switched off.

This feature can be used to pick-up subtitles and display them as OSD anywhere on the screen. An example for building the subtitle mode is given in the section“Example of making the subtitle mode” on page 70.

9.5 Positioning settings

The SAB9077 provides several registers to change the display position of the main- and sub channel PIP on the television screen.
The priority bit decides in cases the Main- and sub channel PIP overlap, which PIP will be on top.
Also several bits for changing the position of the picture inside the PIPs are provided.

9.5.1 Main and sub channel display position

Adjustment of the position of the main- or sub channel PIP can be done with the bits MDhfp, SDhfp, MDhfp and SDvfp. The position of the PIP can be changed to a position anywhere on the screen.

XDhfp	Horizontal fine positioning in 256 steps of 4 pixels each.
XDvfp	Vertical fine positioning in 256 steps of 1 line/field.

The setting of the display position is restricted.

- Horizontal display position restrictions:

The range of the horizontal display position is restricted. This range is influenced by the PIP size

Red. Fact. Single PIP mode H, V	Range Display Position
Q 1/2, 1/2	00 - 76 H
L 1/3, 1/3	00 - 92 H
S 1/4, 1/4	00 - 9E H

Table 13: PIP size and resulting horizontal display position range

If settings are made outside the range given for that Single PIP mode, the picture will be distorted.
The PIP then overlaps the horizontal sync pulse of the display part, what causes picture distortion.

- Vertical display position restrictions:

For the vertical display position there are no restrictions. Vertically the picture can be placed all over the television screen.
If the picture is moved downwards, coming at the bottom, the lower lines of the picture will disappear at the bottom and appear at the top. The picture keeps stable.

Special attention should be given to the situation, when the main channel PIP and the sub channel PIP overlap each other.
The priority of which PIP is on top, can be set with the priority bit, See “Priority bit” on page 36.
If the horizontal and vertical display reduction factors are bigger than 1/2, the pictures inside both PIPs will be distorted in case of overlap. The SAB9077 then has too less time to get all the data out of the VDRAM in time. The data transfer mode should be changed to a 6 bit mode. See the section Data transfer settings.

9.5.2 The Priority bit

The priority bit decides whether the main channel PIP or the sub channel PIP will be on top, when both PIPs overlap. The bit is called PRIO.

PRIO = 0	Priority is given to the sub channel, so the sub channel will be placed on top.
PRIO = 1	Priority is given to the main channel, so the main channel will be placed on top.

The priority bit also influences the border priority.

PRIO = 0	Priority is given to the sub channel borders.
PRIO = 1	Priority is given to the main channel borders.

9.5.3 Main and sub channel acquisition position

Adjustment of the position of the main- or sub channel picture inside the PIP can be done with the bits MAhfp, SAhfp, MAhfp and SAvfp.

XAhfp	Horizontal fine positioning in 16 steps.
XAvfp	Vertical fine positioning in 256 steps of 1 line/field.

The magnitude of the steps, in which the horizontal acquisition position can be moved varies with the horizontal reduction factor.

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Horizontal acq reduction factor	Magnitude of one step
1/1	4 pixels
1/2	2 pixels
1/3	4/3 pixels
1/4	1 pixel

Table 14: Horizontal acq. reduction factor and resulting magnitude of one step for the horizontal acquisition fine-positioning

9.6 Decoder settings

The SAB9077 provides a set of functions to interface not only with the Philips decoder TDA8315, but also with other types of decoders. This means also that different decoders for the main and the sub channel can be used.
The decoder settings can be divided into two parts:

1. Requirements of the analog input signals.
2. Digital decoder settings made inside the SAB9077.

9.6.1 Requirements of the analog input signals

The SAB9077 needs analog input signals for the main channel as well as for the sub channel.
The signals needed are Y, U, V, H-sync and V-sync signals from the decoder. These signals should meet the specs explained in this section

9.6.1.1 Y, U and V signal

There are two modes in which the SAB9077 can be used. The mode that is used depends on the sate of pin 22 TM_2. When pin TM_2 is connected to Vss, the SAB9077 is in the multistandard mode. When pin TM_2 is connected to Vdd, the SAB9077 is in the NTSC mode.The Y, U and V input signal levels for the modes must be:

1. Pin TM_2 = Vss, multistandard mode:
Y = 1 Vpw-pb (peak white - peak black) = 1.4 Vpp
U = 1.33 Vpp
V = 1.05 Vpp

In order to make optimum use of the swing of the ADC of the SAB9077, internally the Y, U and V signals are amplified to input levels of 1.5 Vpp.

The input signal may be PAL as well as NTSC. The use of a multistandard decoder, like the TDA8310, makes the system flexible with regard to the input signals.

2. Pin TM_2 = Vdd, NTSC mode:
Y = 1.5 Vpw-pb (peak white - peak black) = 2.1 Vpp
U = 1.5 Vpp
V = 1.5 Vpp

The Y, U and V input signal levels must be 1,5 Vpp, in order to make optimum use of the swing of the ADC of the SAB9077. This means for the Y-signal that the peak white - peak black level is 1.5 V (Y = 1.5 Vpw-pb).

The ADC conversion range is limited by the voltage across the ADC-resistor-ladder. The top- and bottom levels are respectively Vreft and Vrefb. The level of Vreft is set at 2.1Vdc, the level of Vrefb is set at 0.4 Vdc.
So to make optimum use of the swing of the ADC, the input signal level can be calculated with:
Input signal level = Vreft - Vrefb - Input margin = 1.5 Vpp.
So the input signal level should be 1.5 Vpp, with an input margin of 0.2 V.

9.6.1.2 H-sync signal

The SAB9077 is able to use a H-sync signal as well as a burstkey signal as the horizontal reference pulse. Adjustment of which signal will be used for horizontal synchronisation for the main- and sub channel is possible with the MHSync and SHSync bits of the IIC register (See 9.6.2“Digital decoder settings” on page 41).
Adjustment of which signal will be used for horizontal synchronisation of the display channel is possible with the DHSync bit of the IIC register (See 9.10.4.1 “H-sync timing” on page 82).

The difference in timing between the H-Sync and the burstkey signal is shown in figure 12 “Difference in timing between H-Sync and burstkey” on page 40.
The burstkey signal is made from the burst of the CVBS signal, so the timing is exactly the same as the burst timing in the CVBS signal.

The H-sync signals (and the V-sync signals) are the timing references for the acquisition-window. The acquisition window presents the area where data is sampled and actively processed.

The time base for the digital control is provided by an own PLL for the main, sub and display channel. The H-sync or the burstkey signal is the input signal for the PLL. The PLL will lock at this signal, and produce a steady internal clock of 27 MHz.

The H-sync or burstkey signal should be a normal 5 V pulse, of which the rise- and fall- time should be as small as possible (<<100 nS).
The rising as well as the falling flank should be clean, that means free from noise, ringing etc.

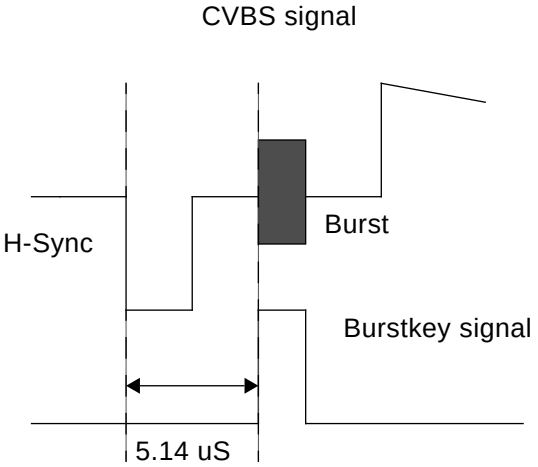


Figure 12: Difference in timing between H-Sync and burstkey

9.6.1.3 V-sync

The SAB9077 needs a positive edge V-sync signal of 5 Vpp as input signal.
Inside the SAB9077 the polarity of the V-sync signal can be adjusted, so also a negative edge V-sync signal can be used.

The polarity of the V-sync signal can be adjusted with the bits MVSync and SVSync (see digital decoder settings).
The polarity of the V-sync signal for the display channel can be adjusted with the bits DVSyn (See 9.10.4.2 “Vertical sync polarity” on page 82).

The V-sync signal should be a normal 5 V pulse, of which the rise- and fall- time should be as small as possible (<<100 nS).
The rising as well as the falling flank should be clean, that means free from noise, ringing etc.

9.6.2 Digital decoder settings

The digital decoder settings enable the use of other decoders than the TDA8315. Several settings can be changed to allow other kinds of inputs. The settings are:

1. H-sync timing
2. Vertical Filter
3. V-sync Polarity
4. Field ID
5. Original UV
6. Non interlace for main and sub
7. 1 Field
8. PAL/NTSC input signal switch

9.6.2.1 H-sync timing

The SAB9077 is able to use a H-sync signal as well as a burstkey signal as the horizontal reference pulse. Adjustment of which signal will be used for horizontal synchronisation is possible with the MHSync and SHSync bits of the IIC register.

XHSync = 0	Synchronize on the burstkey signal.
XHSync = 1	Synchronize on the H-sync signal.

In the SAB9077 the difference in timing between the H-Sync and the burstkey signal is compensated. The timing difference is equal to 69 clock-cycles of the internal 13.5 MHz clock
This can be seen as offset of 69 clock-cycles for the H-Sync signal.

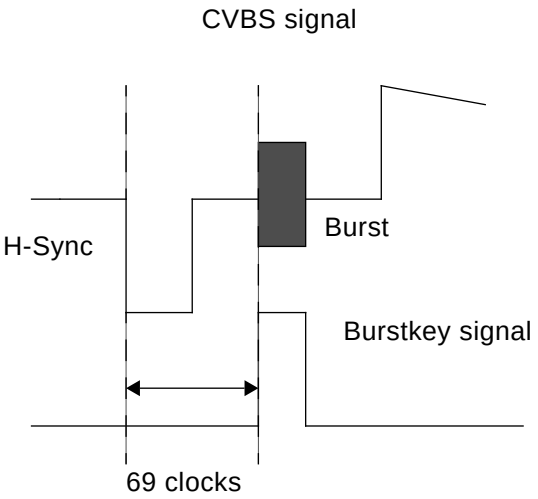


Figure 13: Difference in timing between H-Sync and burstkey

9.6.2.2 Vertical Filter

Better distribution of the lines on the television screen, only in the modes with a vertical reduction factor of 1/3 or 1/4, is offered by the bits MVfilt and SVfilt.
In fact the starting position of the second field is delayed. This improves the vertical frequency response and minimizes aliasing effects.

9.6.2.3 Vertical sync polarity

The active edge of the V-sync signal can be selected with the bits MVSPol and SVSPol.

XVSPol = 0	Positive edge is the active edge.
XVSPol = 1	Negative edge is the active edge.

The decoder used may give a positive as well as a negative V-sync signal as output.

9.6.2.4 Original UV

The SAB9077 is able to invert the polarity of the color difference signals, which are supplied to the main- and sub channel ADC's. The bits MUVPol and SUVPol provide this function.

XUVPol = 0	Positive color difference signals needed as input. This means B-Y, R-Y signals should be supplied.
XUVPol = 1	Negative color difference signals needed as input. This means -(B-Y), -(R-Y) signals should be supplied.

The decoder used may give positive as well as negative color difference signals as output signals.

The settings of XUVPol and DUVPol can be used to invert the whole color difference output signal. XUVPol inverts the color difference signals of the main and sub PIPs. DUVPol inverts the color difference signals of the border and the background.
This means that if the color difference output signals were U and V, the output will be -U, -V.
It does not matter if the stage after the SAB9077 needs U and V input signals or -U and -V input signals.
U is the R-Y color difference signal and V is the B-Y color difference signal.

9.6.2.5 Field polarity

The SAB9077 needs to detect the field identity of the incoming signal to make a correct output signal.

When the fields of the incoming signal are displayed in the wrong order, the picture will be distorted. For example when field 1 of the incoming signal is displayed as field 2 in the SAB9077. and field 2 of the incoming signal as field 1 in the SAB9077, a diagonal straight line will be knurled.

Figure 14: Example of a picture of a straight line, with a normal field id and a twisted field id

The field Id signal is also needed to avoid joint line errors. If a first field is written to the VDRAM, the second field will be read. If the first field is read at the same time that this first field is written to the VDRAM, there will be a point in the picture where old and new data are merged into another. In a moving picture this looks like the picture exists of 2 parts that are slightly shifted from each other.

9.6.3 Non interlace bit for main and sub

The non interlace bits MNonint and SNonint control the interlace mode of the acquisition blocks of the SAB9077. These bits control whether one or two fields in the VDRAM are used to store the video data.

XNonint = 0 Non interlace is internal in the automatic mode. This means that if an interlace signal is detected at the input, the interlace mode will be entered. Now both fields stored in the VDRAM are used by the display part.
Is a non interlace mode detected, the non interlace mode is entered (See DNonint=1).

XNonint = 1 Non interlace is on. One field stored in the VDRAM by the acquisition blocks, but memory for two fields stays allocated.

The XNonint bit overrules the internal automatic interlace detection.

9.6.4 1 Field option

The 1 field bits M1FLD and S1FLD controls the reservation of address spaces in the VDRAM for one or two fields, for the main or the sub channel.

X1FLD = 0	For both fields address spaces are reserved in the VDRAM
X1FLD = 1	For one field address space is reserved in the VDRAM

9.6.5 PAL/NTSC input signal switch

With the bits MPAL and SPAL the SAB9077 can be switched between the NTSC- and PAL standard.

These bits set the acquisition area. When XPAL is set to “1”, the acquisition area is enlarged from 228 lines/field (NTSC standard) to 276 lines/field (PAL standard) vertically. Horizontally the acquisition area is not changed.

XPAL = 0	NTSC standard mode. The acquisition area is 228 lines/field vertically.
XPAL = 1	PAL standard mode. The acquisition area is 276 lines/field vertically.

The PAL/NTSC input signal switch should be set according to the input signal for that channel.

9.7 Channel selection

In the multi-PIP modes each PIP can be filled with a (different) data.Each PIP in a Multi-PIP mode can be selected to show a live picture.
In Multi-PIP modes only one PIP for the main- and one PIP for the sub channel can display a live picture.
The selection of the PIP showing the live picture and/or filling the Multi PIPs with a picture can be done with the bits MLsel and SLsel.

When starting up a multi-PIP mode there are two ways to show the Multi-PIP mode on the television screen:
1. all PIPs can be filled with a 30% gray picture
2. all PIPs can be filled with the previous data from the VDRAM.

The second possibility will not always give a good picture, because the data of the previous PIP mode is still in the VDRAM. Only when switching between two almost identical PIPmodes with the same reduction factors, e.g. Multi-PIP7 and Multi-PIP8, the PIPs can be filled with the previous data.
Notice that in Multi-PIP modes only one PIP for the main- and one PIP for the sub channel can display a live picture. All other PIPs show a frozen picture.

The numbering of the PIPs on the screen has to be explained first, before the channel selection can be explained.

9.7.1 Numbering of the PIPs in Multi PIP modes

The numbering of the PIPs on the screen can be divided into 2 independent numbering:
1. Main channel PIP numbering
2. Sub channel PIP numbering

For both numbering the way of numbering is identical. The numbering starts with PIP 0 at the upper left corner, and ends at the lower right corner. The number of that last PIP depends on the PIP mode chosen.
When the PIPs do not start at the upper left corner, the numbering begins with the PIP that is next in the upper row The next 2 examples explain the PIP numbering

Example 1: Multi-PIP 16 for main (for sub it is the same)

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

Figure 15: numbering of the PIPs

Example 2: Multi-PIP 16 for main and sub
M means main channel PIP
S means sub channel PIP

S 0	M 0	S 1	M 1
M 2	S 2	S 3	M 3
S 4	S 5	S 6	M 4
M 5	M 6	M 7	M 8

Figure 16: Mixed MP16

9.7.2 Selection of the PIP showing a live picture

In Multi PIP modes one PIP can show a live picture, one PIP for the main channel and one PIP for the sub channel. This PIP showing a live picture can be chosen with the bits MLsel and SLsel. The PIP showing a live picture for main and sub can also be chosen independently.

XLsel	PIP selected
0 H	0
1H	1
2 H	2
3 H	3
4 H	4
5 H	5
6 H	6
7 h	7
8 H	8
9 H	9
A H	10
B H	11
C H	12
D H	13
E H	14
F H	15

Table 15: XLsel and the PIP that will be selected

Also when a PIP mode is build, it is necessary that every PIP in this PIP mode can be filled with a (different) picture. To fill a PIP do the following.

1. Select the signal for a certain PIP, with the tuner or the decoder
2. Wait till the tuner or decoder locks with this signal
3. Select the PIP (with the bits MLsel and SLsel).
4. Set the PIP in freeze (with the bits MFreeze and SFreeze)
5. Select the signal for the next PIP, with the tuner or the decoder

6. Wait till the tuner or decoder locks with this signal
7. Select the PIP (with the bits MLsel and SLsel)
8. Set the PIP in freeze (with the bits MFreeze and SFreeze)
9. Repeat 5, 6, 7 and 8 till all PIPs of the PIP mode are filled.

When the loop described in the points 1-9 is not stopped after all PIPs are filled, the PIPs will be updated with new data.
Take care that the value of the bits MLsel does not become bigger than the number of PIPs - 1 for main in the used multi PIP mode. Also take care that the value of the bits SLsel does not become bigger than the number of PIPs - 1 for sub in the used multi PIP mode.
If the value of MLsel or SLsel becomes too big the data in the VDRAM will be distorted and the picture on the screen will also be distorted.

9.7.3 Fill PIPs with 30% gray picture

With the bit FILLOFF the selection between filling the PIPs with a 30% gray picture or with the previous data from the VDRAM is made.

FILLOFF = 0	All PIPs are filled with a 30% gray picture, until their channels are updated. Only exception is the PIP displaying the live picture.
FILLOFF = 1	The PIPs always show the contents of the VDRAM. When the Multi-PIP modes differ to much, distortion will be seen on the screen.

Normally this mode is not used. It can be used when in a television set the television channels are not all selected and a PIP mode is choosen. The channels that should give a noisy picture can now be filled with a 30% gray picture.

9.7.4 Example of channel selection with Multi-PIP 16

In this part a example of channel selection for the Multi-PIP16 mode in PAL will be given.
The IIC slave address of the SAB9077 is 2C H(exadecimal). This address will not be repeated in every step of the channel selection.

1. Selecting the PIP mode.

First the current PIP functions have to be deactivated, and the PIP mode has to be changed to MP16. In this mode on the screen 16 main PIPs will show up. Change the PIP mode with the bits $PiPMode_{(3:0)}$. Of course the main PIP should be switched on with the bit MPIPON and the and sub PIP should be switched of with the bit SPIPON.

Sub Address	Data
00 H	85 H

Table 16: IIC setting

2. Select PAL standard for main- and display channel

The main input select switch should be set to PAL with the bit MPAL. The display output signal switch should be set to PAL

Sub Address	Data
20 H	60 H

Table 17: IIC setting

3. Set the reduction factors

The display reduction factors as well as the acquisition reduction factors must be set for the main channel. Set display- and acquisition reduction factors to 1/4 horizontally and 1/4 vertically.

Display reduction factors

Sub Address	Data
08 H	00 H

Table 18: IIC setting

Acquisition reduction factors

Sub Address	Data
09 H	00 H

Table 19: IIC setting

4. Set border color and brightness for the sub channel

The border color and brightness should be selected. For this example the color green and brightness 70% is chosen.

Sub Address	Data
10 H	64 H

Table 20: IIC setting

5. Set border select color and brightness for the sub channel

The border select color and brightness should be selected. For this example the color red and brightness 100% is chosen.

Sub Address	Data
10 H	72 H

Table 21: IIC setting

6. Set border-size

The border-size should be selected. For this example the border-size is 4 pixels horizontally and 2 lines vertically.

Sub Address	Data
0F H	22 H

Table 22: IIC setting

7. Select the first sub PIP (= 0) with $MLsel_{(3:0)}$.In picture 17 the order of the PIPs is showed.

Sub Address	Data
0D H	00 H

Table 23: IIC setting

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

Figure 17: numbering of the PIPs in MP9

8. Wait till tuner and/or decoder have locked on the input signal

9. Freeze the first main PIP, with the bit MFreeze.The data in the second part of the 00H register may not change because otherwise another PIP mode will be entered.

Sub Address	Data
00 H	A5 H

Table 24: IIC setting

10. Select the second sub PIP (= 1).

Sub Address	Data
0D H	10 H

Table 25: IIC setting

11. Unfreeze the first main PIP, with the bit MFreeze.The data in the second part of the 00H register may not change because otherwise another PIP mode will be entered.

Sub Address	Data
00 H	85 H

Table 26: IIC setting

12. Wait till tuner and/or decoder have locked on the input signal

13. Freeze the second main PIP, with the bit MFreeze.The data in the second part of the 00H register may not change because otherwise another PIP mode will be entered.

Sub Address	Data
00 H	A5 H

Table 27: IIC setting

14. Repeat the steps 9, 10, 11 and 12, till all sub 16 PIPs are filled with a picture of the main decoder.

Notice:

- The time that must be waited to let the decoder and/or tuner lock on the new source signal, depends on the type of decoder, the type of tuner and the configuration that are used.
  There are 3 configurations.

  1- Using 1 decoder and 1 tuners.

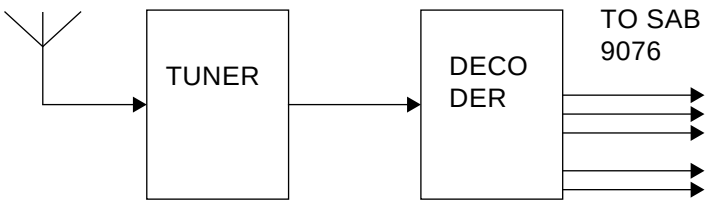


Figure 18: Using 1 decoder and 1 tuner

The time that must be waited for locking on a new source is: Lock-time tuner + lock-time decoder.

2- Using 1 decoder and 2 tuners.

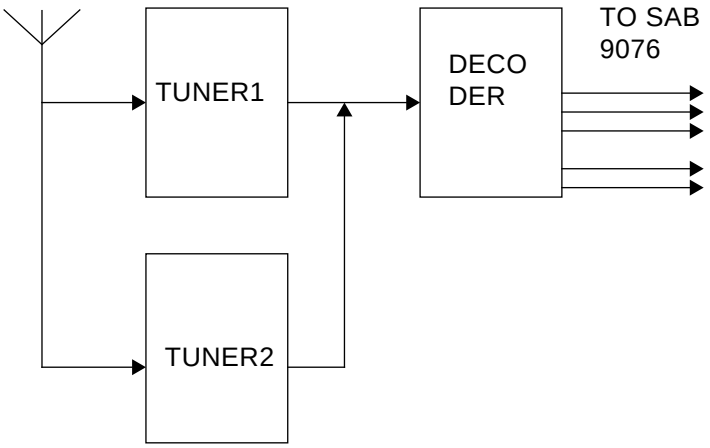


Figure 19: Using 1 decoder and 2 tuner

The time that must be waited for locking on a new source is: lock-time decoder.
The tuner that is not used in the signal path, must lock on the “next needed” source.

3- Using 2 decoder and 2 tuners.

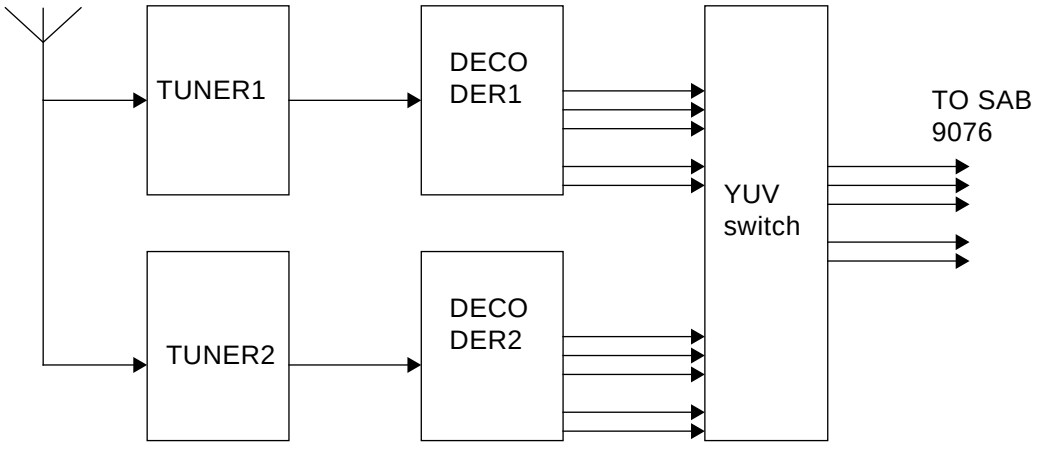


Figure 20: Using 2 decoder and 2 tuner

The time that must be waited for locking on a new source is: no lock-time
The tuner and decoder that are not used in the signal path, must lock on the “next needed” source.

- If the input signals are NTSC, and the output signal should also be NTSC, the bits DPAL and MPAL should both be set to “0”.

Sub Address	Data
20 H	00 H

Table 28: IIC setting

- If the main input signals is NTSC, and the output signal should be PAL, the bits DPAL and MPAL should be set.

The main input select switch should be set to NTSC with the bit SPAL. The display output select switch should be set to PAL with the bit DPAL

Sub Address	Data
20 H	50 H

Table 29: IIC setting

- If the main input signals is PAL, and the output signal should be NTSC, the bits DPAL and MPAL should be set.

The main input select switch should be set to PAL with the bit SPAL. The display output select switch should be set to NTSC with the bit DPAL

Sub Address	Data
20 H	20 H

Table 30: IIC setting

- The sequence can be repeated till a new command is coming from the remote control. Repeating the sequence will refresh the pictures in the sub PIPs.

9.8 Manual mode

In the manual mode more PIP modes become available.With the IIC registers 20H - 32H PIP modes can be build to most pictures one wishes. The manual mode is entered by setting the bits PiPMode in register 00 to 08 H.

The relations between the control-bits are shown in figure 21. The background has a fixed size and can be fine positioned with BGhfp and BGvfp. The shown PIPs are only for one channel (Main or Sub), the other channel is has the same control and can be displayed at the same time.
The PIP mode is build up of maximum of 4 horizontal rows. The minimum is 1 row
Every row is build up of a maximum of four PIPs. The minimum is one PIP.

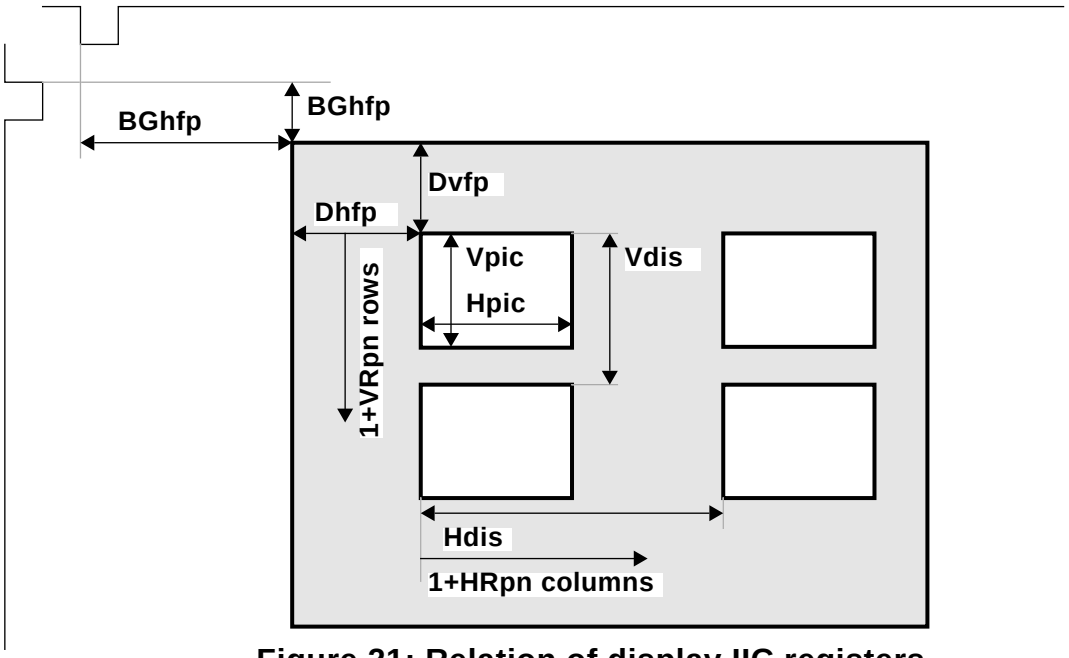


Figure 21: Relation of display IIC registers

According to figure 21 for building a PIP mode the following settings have to be done:

1. Horizontal and vertical picture size
2. Number of rows
3. Number of PIPs in a row
4. Distances between the PIPs horizontally as well as vertically
5. Horizontal offset for a row.

All these settings have to be made in the subaddress registers 20H - 32 H.

The numbering of the PIPs in the PIP mode that is build, is explained in section“Numbering of the PIPs in Multi PIP modes” on page 46

9.8.1 Picture size

The horizontal and vertical picture size can adjusted with the bits MHPic, MVPic, SHPic and SVPic.

Horizontal picture size	XHPic : 256 steps of 4 pixels.
Vertical picture size	XVPic : 256 steps of 1 line/field, when XPAL is set to NTSC.
	XVPic : 256 steps of 2 lines/field, when XPAL is set to PAL.

The Hex values of the standard sizes are listed in table 31.

Size	XHPic	XVPic
1/4	2A H	39 H
1/3	38 H	4C H
1/2	54 H	72 H
1/1	A8 H	E4 H

Table 31: Picture size and corresponding settings for XHPic and XVPic

The hex value of XHPic and XVPic must be >0, otherwise the picture will be distorted.

The maximum hex value for XHPIC is C8. If this value is choosen greater than c8, the picture will be distorted, because the picture interferes with the horizontal sync.

9.8.2 Number of rows

Vertically the number of rows can be selected with the bits MVRpN and SVRpN. Maximum number of rows is 4, minimum is 1.

Rows	XVRpN	
1	0	0
2	0	1
3	1	0
4	1	1

Table 32: Number of rows and corresponding settings for XVRpN

9.8.3 Number of PIPs in a row

Horizontally the number of PIPs in a row can be selected with the bits MHRpOY and SHRpOY. Maximum number of PIPs in one row is 4, minimum is 1. If no PIP should be visible the PIP channel must be switched off (Sub Address 00, bit 7 or 6).

The number of PIPs in a row can be selected for every row, see table 31.

Number of PIPS in Row Y	XHRpOY	
1	0	0
2	0	1
3	1	0
4	1	1

Table 33: Number of PIPs in a row and corresponding settings for XVRpOY

9.8.4 Distances between the PIPs

The horizontal and vertical distance between two successive PIPs can be adjusted.

For each row the distance between starting points of PIPs can be set with the registers $MHDis_n$ and $SHDis_n$ in 256 steps of 4 pixels. Maximum is 1024 pixels.

If settings are made outside the range given for that Single PIP mode, the picture will be distorted.
The PIP then overlaps the horizontal sync pulse of the display part, what causes picture distortion.

The distance between two rows can be set with the MVdis and SVDis registers in 256 steps of 1 line. Maximum is 256 lines/field.

In table 35, standard settings for the horizontal and vertical picture size are shown.

Size	XHPic	XVPic
1/4	2A H	39 H
1/3	38 H	4C H
1/2	54 H	72 H
1/1	A8 H	E4 H

Table 34: Standard settings for XHPIC and XVPIC.

The setting of the distance between the PIPs is restricted.

- Horizontal distance restrictions:

The range of the horizontal distances between the PIPs is restricted. This range is influenced by the number of PIPs in a row.

Red. Fact. Single PIP mode H, V	Range Distance between PIPs	XHRpOY
Q 1/2, 1/2	00 - 76 H	1
L 1/3, 1/3	00 - 92 H	1
L 1/3, 1/3	00 - 4A H	2
S 1/4, 1/4	00 - A2 H	1
S 1/4, 1/4	00 - 4C H	2
S 1/4, 1/4	00 - 32 H	3

Table 35: Range of the horizontal distance between the PIPs in single PIP modes

- Vertical display position restrictions:

The only restriction in the vertical direction is, that the PIP(s) disappear when the vertical distance is set to 0.

9.8.5 Horizontal offset for a row

The horizontal (repetition) offset can be adjusted independently for each row, for the main and for the sub channel.
The offset is adjusted with the bits MHRpOn and SHPpOn.
The offset is very strong related to the horizontal distance. With the horizontal distance adjustment for each row a grid of starting points is created for the PIPs in that row. Every grid point has a number 0 (most left

PIP), 1, 2 or 3. The horizontal (repetition) offset determines the grid number, where the first PIP of that row will be displayed.
In fact a offset for the first PIP is created, and the width of this offset is determined by the horizontal distance.

H Offset	XHRpOn	
0	0	0
1	0	1
2	1	0
3	1	1

Table 36: Horizontal offset and the corresponding settings for XHRpOn

9.8.6 Example of making the Multi-PIP1-12 mode

In this part a example of channel selection for the Multi-PIP1-12 mode, see figure 22, in PAL will be given. The IIC slave address of the SAB9077 is 2C H(exadecimal). This address will not be repeated in every step of the channel selection.

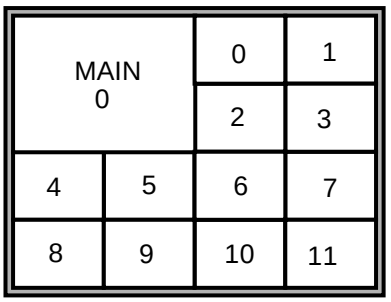


Figure 22: the MP1-12

1. Selecting the PIP mode

First the current PIP functions have to be deactivated, and the PIP mode has to be changed to the manual mode. Also the main channel PIP and sub channel PIP should be switched ON.Change the PIP mode with the bits $PiPMode_{(3:0)}$.

Sub Address	Data
00 H	C8 H

Table 37: IIC setting

2. Select PAL standard for main-, sub- and display channel

The main- and sub input select switch should be set to PAL with the bits MPAL and SPAL. The display output signal switch should be set to PAL

Sub Address	Data
20 H	70 H

Table 38: IIC setting

3. Set main channel PIP and sub channel PIP to 1 field, and sub channel PIP to non interlace.

The main channel PIP and the sub channel PIP should be set to the 1 field mode. Set the bits M1FLD and S1FLD.
The sub channel PIP should be set to the 1noninterlace mode. Set the bit SNonint.

Sub Address	Data
01 H	31 H

Table 39: IIC setting

4. Set the size settings for the sub channel

The horizontal and vertical size of the sub channel can be set with the bits SHPic and SVPic. These bits should both be set to 1/4 for the Multi-PIP 1-12 mode.

Horizontal size

Sub Address	Data
2C H	2A H

Table 40: IIC setting

Vertical size

Sub Address	Data
2D H	39 H

Table 41: IIC setting

5. Set number of rows for the sub channel

Now the number of rows should be set according to the PIP mode, that is going to be build.
The number of rows can be set with the bit SVRpN. For the Multi-PIP 1-12 mode the number of rows for the sub channel PIP is 4.

Sub Address	Data
20 H	73 H

Table 42: IIC setting

6. Set number of PIPs in the rows for the sub channel

The number of PIPs in the rows for the sub channel should be set according to the PIP mode, that is going to be build.
The number of rows can be set with the bits SHRpNY. For the Multi-PIP 1-12 mode the number of PIPs in row Y is displayed in table 31.

Row Y	Number of PIPs	SHRpNY	
1	2	1	0
2	2	1	0
3	4	1	1
4	4	1	1

Table 43: IIC setting

The data that should be send to the Subaddress 2B H is displayed in table 44

Sub Address	Data
2B H	F5 H

Table 44: IIC setting

7. Set the horizontal offset for the sub channel rows.

The horizontal offset for the PIPs in one row should be set. For each row, in this case 4, the horizontal offset can be set, with the bits SHRpOY. The horizontal offset for the 4 rows is displayed in table 31.

Row Y	Offset
1	2
2	2
3	0
4	0

Table 45: IIC setting

The data that should be send to the sub address 2AH is displayed in table 44

Sub Address	Data
2B H	0A H

Table 46: IIC setting

8. Set the vertical distances for the sub channel columns.

The vertical distances for the PIPs in one column should be set. The vertical distance can be set with the bits SVDis, and is the same for each column.

The data that should be send to the sub address 32H is displayed in table 44.

Sub Address	Data
32 H	39 H

Table 47: IIC setting

9. Set the display position for the sub channel

The horizontal and vertical display position of the sub channel PIP should be set.

Horizontal display position

Sub Address	Data
04 H	05 H

Table 48: IIC setting

Sub Address	Data
05 H	03 H

Table 49: IIC setting

10. Set border color and brightness for the sub channel

The border color and brightness should be selected. For this example of the Multi-PIP 1-12 mode the color blue and brightness 100% is chosen.

Sub Address	Data
10 H	71 H

Table 50: IIC setting

11. Set border select color and brightness for the sub channel

The border select color and brightness should be selected. For this example of the Multi-PIP 1-12 mode the color red and brightness 100% is chosen.

Sub Address	Data
11 H	72 H

Table 51: IIC setting

12. Set border-size

The border-size should be selected. For this example of the Multi-PIP 1-12 mode the border-size is 4 pixels horizontally and 2 lines vertically.

Sub Address	Data
0F H	22 H

Table 52: IIC setting

13. Set the size settings for the main channel

The horizontal and vertical size of the main channel can be set with the bits MHPic and MVPic. These bits should both be set to 1/2 for the Multi-PIP 1-12 mode.

Horizontal size

Sub Address	Data
2C H	54 H

Table 53: IIC setting

Vertical

Sub Address	Data
2D H	72 H

Table 54: IIC setting

14. Set the display position for the main channel

The horizontal and vertical display position of the main channel PIP should be set.

Horizontal display position

Sub Address	Data
06 H	03 H

Table 55: IIC setting

Vertical display position

Sub Address	Data
07 H	05 H

Table 56: IIC setting

15. Set the acquisition position for the main- and sub channel

The horizontal and vertical acquisition position of the main- and sub channel PIP should be set. The horizontal acquisition position for the main- and sub channel can be set in the same register.

Horizontal acquisition position for main and sub channel

Sub Address	Data
0A H	00 H

Table 57: IIC setting

Vertical acquisition position for the main channel

Sub Address	Data
0C H	18 H

Table 58: IIC setting

Vertical acquisition position for the sub channel

Sub Address	Data
0B H	18 H

Table 59: IIC setting

16. Select the first sub PIP with $SLsel_{(3:0)}$.In picture 17 the order of the PIPs is showed.
In the same register the main PIP can be selected to be live.

Sub Address	Data
0D H	00 H

Table 60: IIC setting

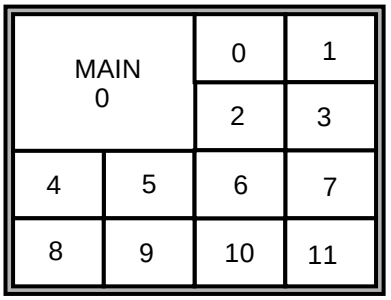


Figure 23: Numbering in the MP1-12

17. Wait till tuner and/or decoder have locked on the input-signal

18. Freeze the first sub PIP, with the bit sFreeze.The data in the second part of the 00H register may not change because otherwise another PIP mode will be entered.

Sub Address	Data
00 H	D8 H

Table 61: IIC setting

19. Select the second sub PIP.

Sub Address	Data
0D H	01 H

Table 62: IIC setting

20. Unfreeze the first sub PIP, with the bit SFreeze.The data in the second part of the 00H register may not change because otherwise another PIP mode will be entered.

Sub Address	Data
00 H	C8 H

Table 63: IIC setting

21. Wait till tuner and/or decoder have locked on the input-signal

22. Freeze the second sub PIP, with the bit SFreeze.

Sub Address	Data
00 H	D8 H

Table 64: IIC setting

23. Repeat the steps 18, 19, 20 and 21, till all sub PIPs are filled with a picture of the sub decoder.

Notice:

- The time that the decoder and or tuner need to lock to the video input signal depends on the type of decoder and/or tuner and the configuration used. See note at page 49
- If the input signals are NTSC, and the output signal should also be NTSC, the bits DPAL, SPAL and MPAL should be set to “0”.

Sub Address	Data
20 H	03 H

Table 65: IIC setting

- If the main input signal is PAL, and the sub input signal is NTSC, there are two settings that can be made for the display input signal switch. The display input signal switch can be set to PAL or NTSC.

  1-: Display input signal switch: PAL

  (Main is PAL and sub is NTSC)

  The bits DPAL, SPAL and MPAL should be set to “1”, “0” and “1”. The other data of the register should stay the same.

Sub Address	Data
20 H	63 H

Table 66: IIC setting

The sub picture will show “too much” lines, because a NTSC picture contains (276 - 228 =) 48 lines less than a PAL picture.
The NiPCoff bit determines whether a grey bar is inserted in case a NTSC PIP is displayed in a PIP with PAL PIP size. The missing lines are equally divided between the top part and the bottom part of the PIP window and made 30% grey. If this bit is ‘0’ the grey bar is displayed, if this bit is ‘1’ the grey bar is omitted and the PIP data is shifted up.

Set the NiPCoff bit to “1”

Sub Address	Data
01 H	3A H

Table 67: IIC setting

2-: Display input signal switch: NTSC
(Main is PAL and sub is NTSC)

The bits DPAL, SPAL and MPAL should be set to “0”, “0” and “1”. The other data of the register should stay the same.

Sub Address	Data
20 H	23 H

Table 68: IIC setting

The main picture will show “loose” 48 lines, because a PAL picture contains (276 - 228 =) 48 lines more than a NTSC picture.

- If the main input signal is NTSC, and the sub input signal is PAL, there are two settings that can be made for the display input signal switch. The display input signal switch can be set to PAL or NTSC.

1-: Display input signal switch: PAL

(Main is NTSC and sub is PAL)

The bits DPAL, SPAL and MPAL should be set to “1”, “1” and “0”. The other data of the register should stay the same.

Sub Address	Data
20 H	53 H

Table 69: IIC setting

The main picture will show “too much” lines, because a NTSC picture contains (276 - 228 =) 48 lines

less than a PAL picture.
The NiPCoff bit determines whether a grey bar is inserted in case a NTSC PIP is displayed in a PIP with PAL PIP size. The missing lines are equally divided between the top part and the bottom part of the PIP window and made 30% grey. If this bit is ‘0’ the grey bar is displayed, if this bit is ‘1’ the grey bar is omitted and the PIP data is shifted up.

Set the NiPCoff bit to “1”

Sub Address	Data
01 H	3A H

Table 70: IIC setting

2-: Display input signal switch: NTSC
(Main is NTSC and sub is PAL)

The bits DPAL, SPAL and MPAL should be set to “0”, “1” and “0”. The other data of the register should stay the same.

Sub Address	Data
20 H	13 H

Table 71: IIC setting

The sub picture will show “loose” 48 lines, because a PAL picture contains (276 - 228 =) 48 lines more than a NTSC picture.

- The sequence can be repeated till a new command is coming from the remote control. Repeating the sequence will refresh the pictures in the sub PIPs.

9.8.7 Example of making a 16:9 PIP

In this section the making of a 16:9 picture for the sub channel is explained. This PIP will be placed in the original live picture, what means that the background will be switched off. See figure .
Both signals are PAL standard signals.
The IIC slave address of the SAB9077 is 2C H(exadecimal). This address will not be repeated in every step of the channel selection.

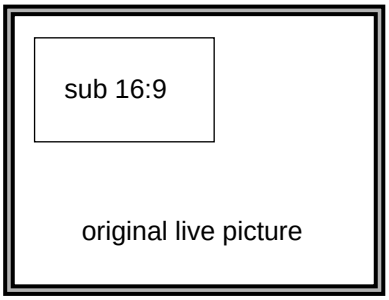


Figure 24: 16:9 PIP

1. Selecting the PIP mode

First the current PIP functions have to be deactivated, and the PIP mode has to be changed to the manual mode. Also the sub channel PIP should be switched ON.Change the PIP mode with the bits $PiPMode_{(3:0)}$.

Sub Address	Data
00 H	48 H

Table 72: IIC setting

2. Select PAL standard for, sub- and display channel

The sub input select switch should be set to PAL with the bit SPAL. The display output select switch should be set to PAL with the bit DPAL

Sub Address	Data
20 H	50 H

Table 73: IIC setting

3. Set the size settings for the sub channel

The horizontal and vertical size of the sub channel can be set with the bits SHPic and SVPic. These bits should both be set so that a 16:9 picture will appear. For example when the horizontal size is 1/2, the vertical size should be 72 lines/field.

Horizontal size

Sub Address	Data
2C H	72 H

Table 74: IIC setting

Vertical size

Sub Address	Data
2D H	68 H

Table 75: IIC setting

4. Select the sub PIP with $SLsel_{(3:0)}$ to make the PIP showing a live picture.

Sub Address	Data
0D H	00 H

Table 76: IIC setting

5. Set border color and brightness for the sub channel

The border color and brightness should be selected. For this example of the 16:9 PIP mode the color green and brightness 70% is chosen.

Sub Address	Data
10 H	64 H

Table 77: IIC setting

6. Set border-size

The border-size should be selected. For this example of the Multi-PIP 1-12 mode the border-size is 4 pixels horizontally and 2 lines vertically.

Sub Address	Data
0F H	22 H

Table 78: IIC setting

7. Switch background off

The background can be switched OFF by setting the bit BGON to 0.

Sub Address	Data
14 H	00 H

Table 79: IIC setting

notice:

- **Using NTSC input signals for sub- and display channel**

When NTSC input signals are used for the sub- and display channel, some registers need other data. The changes in the registers are listed below.

1. Select PAL standard for, sub- and display channel

The sub input select switch should be set to NTSC with the bit SPAL. The display output select switch should be set to NTSC with the bit DPAL

Sub Address	Data
20 H	00 H

Table 80: IIC setting

2. Set the size settings for the sub channel

The horizontal and vertical size of the sub channel can be set with the bits SHPic and SVPic. These bits should both be set so that a 16:9 picture will appear. For example when the horizontal size is 1/2, the vertical size should be 86 lines/field.

Horizontal size

Sub Address	Data
2C H	72 H

Table 81: IIC setting

Vertical size

Sub Address	Data
2D H	56 H

Table 82: IIC setting

- **Using NTSC input signal for the sub channel and PAL input signal for the display channel**

When a NTSC input signal are used for the sub channel and a PAL input signal for the display channel, some registers need other data. The changes in the registers are listed below.

1. Select PAL standard for, sub- and display channel

The sub input select switch should be set to NTSC with the bit SPAL. The display output select switch should be set to PAL with the bit DPAL

Sub Address	Data
20 H	40 H

Table 83: IIC setting

2. Set the size settings for the sub channel

The horizontal and vertical size of the sub channel can be set with the bits SHPic and SVPic. These bits should both be set so that a 16:9 picture will appear. For example when the horizontal size is 1/2, the vertical size should be 86 lines/field.

Horizontal size

Sub Address	Data
2C H	72 H

Table 84: IIC setting

Vertical size

Sub Address	Data
2D H	68 H

Table 85: IIC setting

3. Switch on the NiPCoff bit

The sub picture will show “too much” lines, because a NTSC picture contains (276 - 228 =) 48 lines less than a PAL picture.
The NiPCoff bit determines whether a grey bar is inserted in case a NTSC PIP is displayed in a PIP with PAL PIP size. The missing lines are equally divided between the top part and the bottom part of the PIP window and made 30% grey. If this bit is ‘0’ the grey bar is displayed, if this bit is ‘1’ the grey bar is omitted and the PIP data is shifted up.

Sub Address	Data
01 H	3A H

Table 86: IIC setting

- **Using PAL input signal for the sub channel and NTSC input signal for the display channel**

When a PAL input signals is used for the sub channel and a NTSC input signal for the display channel, some registers need other data. The changes in the registers are listed below.

1. Select PAL standard for, sub- and display channel

The sub input select switch should be set to PAL with the bit SPAL. The display output select switch should be set to NTSC with the bit DPAL

Sub Address	Data
20 H	10 H

Table 87: IIC setting

2. Set the size settings for the sub channel

The horizontal and vertical size of the sub channel can be set with the bits SHPic and SVPic. These bits should both be set so that a 16:9 picture will appear. For example when the horizontal size is 1/2, the vertical size should be 86 lines/field.

Horizontal size

Sub Address	Data
2C H	72 H

Table 88: IIC setting

Vertical size

Sub Address	Data
2D H	56 H

Table 89: IIC setting

The sub picture will “loose” some lines, because a PAL picture contains more lines than a NTSC picture.

9.8.8 Example of making the subtitle mode

The subtitle mode is a special feature of the SAB9077, which can be made in the manual mode. How to make this mode is explained in this section.
Both signals are PAL standard signals.
The IIC slave address of the SAB9077 is 2C H(exadecimal). This address will not be repeated in every step of the channel selection.

1. Selecting the PIP mode.

First the current PIP functions have to be deactivated, and the PIP mode has to be changed to Full Field Still. In this mode on the screen 1 main PIP will show up in the freeze mode. Change the PIP mode with the bits $PiPMode_{(3:0)}$.

Sub Address	Data
00 H	08 H

Table 90: IIC setting

2. Select PAL standard for, main-, sub- and display channel

The main- and sub input select switch should be set to PAL with the bits XPAL. The display output select switch should be set to PAL with the bit DPAL

Sub Address	Data
20 H	70 H

Table 91: IIC setting

3. Settings for main and sub channel PIP.

The following settings must be done regarding the main and sub channel PIP
1-:Switch main channel PIP ON. Set bit MPIPON
2-:Switch sub channel PIP OFF. Set bit SPIPON
3-:Set main channel PIP and sub channel PIP in the freeze mode. Set the bits MFreeze and SFreeze

The setting of the PiPMode must be kept the same.

Sub Address	Data
00 H	C8 H

Table 92: IIC setting

4. Set main- and sub channel PIP to 1 field

The main- and the sub channel PIP should be set to the 1 field mode. Set the bits M1FLD and S1FLD.

Sub Address	Data
01 H	30 H

Table 93: IIC setting

5. Set reduction factors

The reduction factors for main display and acquisition must be set to horizontally 1/1 and vertically to 1/1. This should be done with the bits MDredH, MdredV, MAredH and MAredV.

First set the display reduction factors

Sub Address	Data
08 H	00 H

Table 94: IIC setting

Then set the acquisition reduction factors

Sub Address	Data
09 H	00 H

Table 95: IIC setting

6. Switch background off

the background can be switched OFF by setting the bit BGON to 0.

Sub Address	Data
14 H	00 H

Table 96: IIC setting

7. Switch the main channel PIP to live

The main channel PIP can be switched to live by changing the bit MFreeze to 0.

Sub Address	Data
00 H	A8 H

Table 97: IIC setting

8. Set for the manual mode

For changing to the manual mode the PIP mode has to be changed. This can be done with the bits PiPMode.

Sub Address	Data
00 H	AF H

Table 98: IIC setting

9. Set the sizes of the subtitle

The horizontal and vertical size of the subtitle box have to be adjusted. To arrange this, the display sizes of the main channel PIP must be set, so that the box is big enough to contain the subtitles. With the bits MHpic and MVpic the horizontal and vertical display size can be adjusted.

Horizontal

Sub Address	Data
23 H	FF H

Table 99: IIC setting

Vertical

Sub Address	Data
24 H	0F H

Table 100: IIC setting

The sizes of the subtitle box are now (see picture):
Horizontal 256 x 4 = 1024 pixels. This means the horizontal size is the maximum width.
Vertical 15 x 1 = 15 lines/field. This means the vertical size is 30 lines/frame.

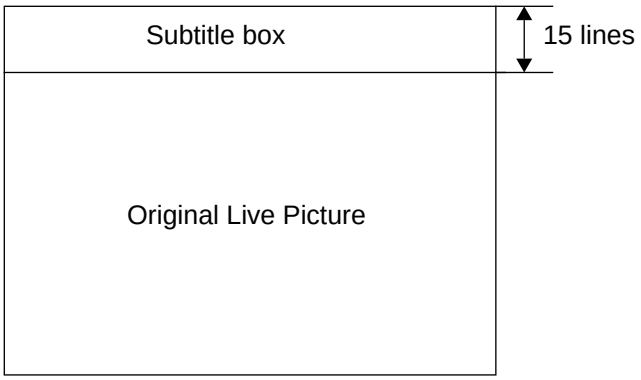


Figure 25: Position of the subtitle box on the television screen

10. Set position of the subtitle box on the screen.

The position of the subtitle box on the screen can be changed with the main channel display positioning.The bits MDhfp and MDvfp must be set.
To set the subtitle box at the bottom of the original live picture, make the following settings.

Horizontal position

Sub Address	Data
06 H	00 H

Table 101: IIC setting

Vertical

Sub Address	Data
07 H	FF H

Table 102: IIC setting

11. Set the acquisition position of the picture in the subtitle box

The acquisition position of the main channel picture inside the subtitle box so, that the subtitle text can be seen in the subtitle box.
For example when the subtitles are at the bottom of the original live picture, the acquisition position should be set as follows.

Horizontal

Sub Address	Data
0A H	00 H

Table 103: IIC setting

Vertical

Sub Address	Data
24 H	E4 H

Table 104: IIC setting

12. Switch the border ON/OFF

The border can be switched ON or OFF with the bits MBON and MBSON.
When only the text of the subtitles are important, the border should be switched OFF.

Switch OFF the border

Sub Address	Data
12 H	00 H

Table 105: IIC setting

13. Switch OFF border select

In the subtitles mode the border select should be switched OFF.

Sub Address	Data
13 H	00 H

Table 106: IIC setting

14. Set the transparency of the subtitle box

The transparency level should be set so, that the subtitle text can be read in the subtitle box and all other irrelevant information is rejected. This means only the subtitle text should be written over the original live picture. If the subtitle text contains white letters, Yth should be set to 12 or 13. Then only the white letters of the subtitles will be displayed in the original live picture. Setting Yth is done with the bit Yth.

Sub Address	Data
02 H	0F H

Table 107: IIC setting

Notice:

- To make a subtitle mode the used PIP (main- or sub channel) must have the same synchronisation as the signal that synchronizes the display part (original live picture).
- It is very important to make the steps for building the subtitle mode in the successive order mentioned above.
- When using NTSC signals for the main- and display channel the XPAL bits should be set to “0”.

Sub Address	Data
20 H	00 H

Table 108: IIC setting

- In the subtitle mode only the PAL/PAL and the NTSC/NTSC mode are possible. Because the original live picture (synchronizes the display part of the SAB9077) must be the same as the main (or sub) picture. Otherwise subtitles that do not belong to the original live picture will be displayed.

9.9 Television standard converter (or transcoder)

The SAB9077 can be used as a television standard converter. It is possible to display a full field PAL standard television signal in a NTSC environment or a NTSC standard television signal in a PAL environment.

9.9.1 Displaying a PAL signal in a NTSC environment

This means that the main- and display channel input signals are NTSC television standard signals, the sub channel input signal is PAL.
In this example for the main- and display channel the same television standard is assumed because in most applications main- and display channel will be connected together.

1. Selecting the PIP mode

First the current PIP functions have to be deactivated, and the PIP mode has to be changed to the manual mode. Also the main channel PIP and sub channel PIP should be switched ON.Change the PIP mode with the bits $PiPMode_{(3:0)}$.

Sub Address	Data
00 H	00 H

Table 109: IIC setting

2. Set the PAL/NTSC standard input select switch for main-, sub- and display channel

The main channel input select switch should be set to PAL with the bit MPAL. The sub channel input select switch should be set to PAL with the bit SPAL. The display output signal switch should be set to PAL

Sub Address	Data
20 H	60 H

Table 110: IIC setting

3. Settings for main- and sub channel PIP.

The following settings must be done regarding the main and sub channel PIP
1-:Switch main channel PIP OFF. Set bit MPIPON
2-:Switch sub channel PIP ON. Set bit SPIPON
3-:Set main channel PIP in the freeze mode. Set the bits MFreeze

The setting of the PiPMode must be kept the same.

Sub Address	Data
00 H	60 H

Table 111: IIC setting

4. Set main channel PIP and sub channel PIP to 1 field, and sub channel PIP to non interlace.

The main channel PIP and the sub channel PIP should be set to the 1 field mode. Set the bits M1FLD and S1FLD.
The sub channel PIP should be set to the 1noninterlace mode. Set the bit SNonint.

Sub Address	Data
01 H	31 H

Table 112: IIC setting

5. Set data transfer mode

The data transfer mode should be set to SMART6

Sub Address	Data
02 H	20 H

Table 113: IIC setting

6. Set the reduction factors

The display reduction factors as well as the acquisition reduction factors must be set for the main channel. Set display- and acquisition reduction factors to 1/4 horizontally and 1/4 vertically.

Display reduction factors

Sub Address	Data
08 H	05 H

Table 114: IIC setting

Acquisition reduction factors

Sub Address	Data
09 H	05 H

Table 115: IIC setting

7. Set the display position for the sub channel

The horizontal and vertical display position of the sub channel PIP should be set.

Horizontal display position

Sub Address	Data
04 H	00 H

Table 116: IIC setting

Sub Address	Data
05 H	00 H

Table 117: IIC setting

8. Set the acquisition position for the sub channel

The horizontal and vertical acquisition position of the main- and sub channel PIP should be set. The horizontal acquisition position for the main- and sub channel can be set in the same register.

Horizontal acquisition position for the sub channel

Sub Address	Data
0A H	00 H

Table 118: IIC setting

Vertical acquisition position for the sub channel

Sub Address	Data
0B H	18 H

Table 119: IIC setting

9. Set horizontal and vertical background position

The horizontal and vertical position of the background should be set (this setting is only for this example).

Sub Address	Data
03 H	99 H

Table 120: IIC setting

10. Set border color and brightness for the sub channel

The border color and brightness should be selected. For this example the color green and brightness 70% is chosen.

Sub Address	Data
10 H	64 H

Table 121: IIC setting

11. Set border-size

The border-size should be selected. For this example the border-size is 4 pixels horizontally and 2 lines vertically.

Sub Address	Data
0F H	22 H

Table 122: IIC setting

notice:

- The displayed PAL picture will be missing 48 lines. It depends on the setting of the vertical acquisition position SAvfp which lines are missing. The lines can be missing at the bottom, half at the top and half at the bottom or at the top.All stages between.

9.9.2 Displaying a NTSC signal in a PAL environment

This means that the main- and display channel input signals are PAL television standard signals, the sub channel input signal is NTSC.
In this example for the main- and display channel the same television standard is assumed because in most applications main- and display channel will be connected together.

The procedure for displaying a NTSC signal in a PAL environment is the same as the procedure for displaying a PAL signal in a NTSC environment. There are some differences which will be explained beneath.

1. The bits DPAL and MPAL should be set to PAL. The bit SPAL should be set to NTSC.

Sub Address	Data
20 H	63 H

Table 123: IIC setting

2. Set the NiPCoff bit to “1”

The sub picture will show “too much” lines, because a NTSC picture contains (276 - 228 =) 48 lines less than a PAL picture.

The NiPCoff bit determines whether a grey bar is inserted in case a NTSC PIP is displayed in a PIP with PAL PIP size. The missing lines are equally divided between the top part and the bottom part of the PIP window and made 30% grey. If this bit is ‘0’ the grey bar is displayed, if this bit is ‘1’ the grey bar is omitted and the PIP data is shifted up.

Sub Address	Data
01 H	39 H

Table 124: IIC setting

9.10 Display settings

The display settings are a set o settings, which have influence on the output signals of the SAB9077. The set contains the settings:

1. D(igital) filter
2. Non interlace bit
3. F(ast) B(lank) Delay
4. Pedestal level U and V
5. Vertical sync polarity (DVSPol)
6. Horizontal sync selection (DHsync)
7. Field ID polarity (DFPol)
8. NiPCoff bit, NTSC-PAL correction factor
9. PAL/NTSC output signal switch

9.10.1 D(igital) filter

The D(igital) filter is an interpolating filter to come from type internal 864 pixel data rate to the output data rate of 2 * 864 pixels. These 2* 864 pixels are converted to an analog signal by the DACs.

Switching the D filter on will improve the picture quality.

DFilt =0 D filter is off. No interpolation to come to the 2*864 pixels data rate.
DFilt =1 D filter is on. Interpolation to come to the 2*864 pixels data rate.

9.10.2 Non interlace bit for the display part

The non interlace bit DNonint controls which fields, stored in the VDRAM are used by the display part of the SAB9077, for the PIPs set on the television screen.

DNonint =0 Non interlace is internal in the automatic mode. This means that if an interlace signal is detected at the input, the interlace mode will be entered. Now both fields stored in the VDRAM are used by the display part.
Is a non interlace mode detected, the non interlace mode is entered (See DNonint=1).

Dnonint =1 Non interlace is on. One field stored in the VDRAM is used by the display part.

The DNonint bit overrules the internal automatic interlace detection.

9.10.3 F(ast) B(lank) Delay

The fast blank delay determines the start-point of the Fast Blank signal. The fast blank signal determines the place where in the original live picture a cut out will be made. The space in this cut out will be filled with the PIP pictures.

With the fast blank delay the delay between the fast blank signal and the PIP signals can be adjusted to zero. The range of the fast blank delay is 8 steps of a half clock-cycle, from -4 to +3. 0H is the mid position.
The relation between the delay times in 1/2 clock-cycles and the FBDel bits is shown in table 125

delay	FBDel 2	FBDel 1	FBDel 0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Table 125: Fast Blank delay and the corresponding settings for FB Delay

delay	FBDel 2	FBDel 1	FBDel 0
-1	1	1	1
-2	1	1	0
-3	1	0	1
-4	1	0	0

Table 125: Fast Blank delay and the corresponding settings for FB Delay

9.10.4 Pedestal level U and V

With the bits PedstU and PedestV the color difference signals U and V, can be adjusted within small limits. The pedestal level settings can be used to adjust the white level of the picture inside the PIPs.

The bits PedstU and PedestV give the U and V DAC an offset of -8 to +7 LSB. 0H is mid-position.

With the pedestal level U the U (B-Y) signal can be adjusted in 16 steps.
With the pedestal level U the U (B-Y) signal can be adjusted in 16 steps.

The system can be adjusted to meet the specifications of the color-temperatures that are used for the television set.
Changing the settings of PedestU and PedestV will change the RGB signal components. When the PedestU is changed, not only the B(lue) signal will change, the G(reen) signal will also change. G(reen) is made out of U and V in the matrix after the SAB9077.

When the PIP is switched off, a non colored black becomes output. This black level can be adjusted

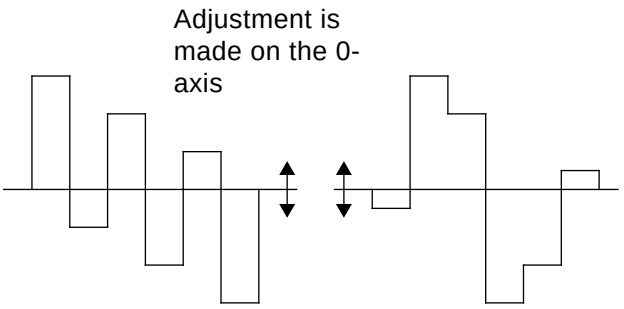


Figure 26: Adjustment of the 0 level of the U and V signal, made with UPedest and VPedest.

9.10.4.1 H-sync timing

The SAB9077 is able to use a H-sync signal as well as a burstkey signal as the horizontal reference pulse. Adjustment of which signal will be used for horizontal synchronisation is possible with the DHSync bit of the IIC register.

DHSync = 0	Synchronize on the burstkey signal.
DHSync = 1	Synchronize on the H-sync signal.

9.10.4.2 Vertical sync polarity

The active edge of the V-sync signal can be selected with the bits DVSPol.

DVSPol = 0 Positive edge is the active edge.
DVSPol = 1 Negative edge is the active edge.

The decoder used may give a positive as well as a negative V-sync signal as output.

9.10.5 Field polarity

The SAB9077 needs to detect the field identity of the incoming signal to make a correct output signal.

When the fields of the incoming signal are displayed in the wrong order, the picture will be distorted. For example when field 1 of the incoming signal is displayed as field 2 in the SAB9077. and field 2 of the incoming signal as field 1 in the SAB9077, a diagonal straight line will be knurled.

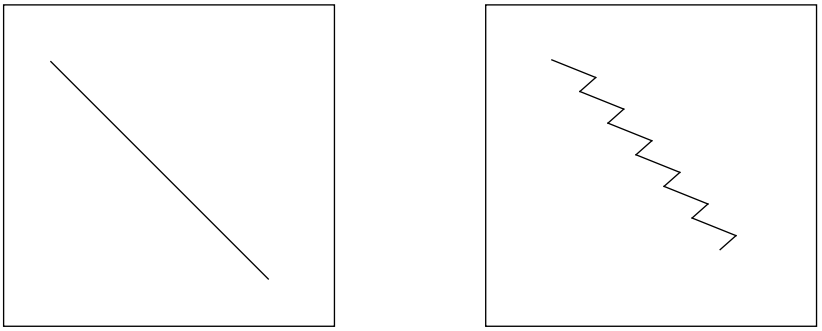


Figure 27: Example of a picture of a straight line, with a normal field id and a twisted field id

The field Id signal is also needed to avoid joint line errors. If a first field is written to the VDRAM, the second field will be read. If the first field is read at the same time that this first field is written to the VDRAM, there will be a point in the picture where old and new data are merged into another. In a moving picture this looks like the picture exists of 2 parts that are slightly shifted from each other.

9.10.6 PAL/NTSC output signal switch

With the bit DPAL the output signal of the SAB9077 can be switched between the NTSC- and PAL standard.

This bit set the display area. When DPAL is set to “1”, the display area is enlarged from 228 lines/field (NTSC standard) to 288 lines/field (PAL standard) vertically. Horizontally the acquisition area is not changed.

DPAL = 0 NTSC standard mode. The display area is 238 lines/field vertically.
DPAL = 1 PAL standard mode. The display area is 288 lines/field vertically.

The PAL/NTSC input signal switch should be set according to the standard of the original live picture for that channel. This means that the television standard of the display part should be the same as the television standard of the deflection part of the television.

9.11 Output settings

The 2* 864 pixels data rate is converted into an analog signal by the 8 bit DACs of the SAB 9076. The output signals are DY, DU and DV, so in other words the output is a component format.

Default signal levels for the output signals DY, DU and DV are 1.5 Vpp. This means that the overall gain of the SAB9077 is 1.

The output signals DY, DU and DV are made low-ohmic by means of the output buffers between the DACs and the output pins.

The output voltages of the DACs are set by the DAVreft and the DAVrefb input voltages.

The output load resistors should be 220 to get the overall gain of 1.

The output buffer has a unit voltage gain and a output resistance of 25 Ohm. So when the load resistance R_l = 220 Ohm, the gain is 220/245.
A unit gain is therefore achieved when the DAC input range equals 245/220 times the ADC input range.
DAC (Vreft - Vrefb) = 245/220 * 1.7 = 1.9 V. So Vreft - Vrefb must be 1.9 V, choose Vrefb = 0.4 V and Vreft = 2.3 V
For the ADC input range see section.

9.12 zoom function

A zoom function for the main- and sub channel PIP can be made by writing a program that is able to change the IIC settings of the SAB9077.
An example of a zoom program is listed below. The program is written in C++.

In this program there are two functions for the main channel zoom. The function zoom_mainup zooms the main picture into the original live picture. This means that after the execution of this function, the main channel PIP can be seen in the original live picture.
The function zoom_maindown zooms the main picture out of the original live picture. This means that after the execution of this function, the main channel PIP can not be seen in the original live picture.

In the same way two functions for the sub channel can be created.

Both functions need data from the IIC registers of the SAB9077 as well as data from the control software that controls the SAB9077.
The data needed from the IIC registers of the SAB9077 are the bits:
MHPIC
MVPIC
MDhfp
MDvfp

The data needed from the control software are:
Zoom on/off
PIP on/off
The number of steps in which the zoom function should be executed (steps).
The direction of the zoom. In this example the direction of the zoom is given by an integer. The directions that can be selected are none, left or centre (hzoom and vzoom).

```
void ZOOM_MainUp(int Hands[])
{
  int init;
  int mhpic, mvpic;
  int mdhfp, mdvfp;
  int hsize, vsize;
  int hpos, vpos:
  int hzoom, vzoom;
  int steps;
  int i;

 GET THE IIC DATA FROM THE SAB9076. THE SETTINGS OF THE FOLLOWING BITS ARE
 NEEDED:
 MHPIC
 MVPIC
 MDhfp
 MDvfp

 GET THE DATA FROM THE CONTROL SOFTWARE. THE FOLLOWING DATA ARE NEEDED:
 Zoom on or off.
```

The number of stepS
The direction of the zoom

```
 init = 1;
   for (i = 5; i < steps; i++) {
      switch ( hzoom ) {
        case ZOOM_None :
              hsize = mhpic;
              hpos  = mdhfp;
           break;
        case ZOOM_Left :
              hsize = (i*mhpic)/(steps);
              hpos  = mdhfp;
           break;
        case ZOOM_Center :
              hsize = (i*mhpic)/(steps);
              hpos  = mdhfp+mhpic/2-(i*mhpic)/(2*steps);
            break;
      }
       switch ( vzoom ) {
        case ZOOM_None :
              vsize = mvpic;
              vpos  = mdvfp;
            break;
        case ZOOM_Left :
              vsize = (i*mvpic)/(steps);
              vpos  = mdvfp;
            break;
        case ZOOM_Center :
              vsize = (i*mvpic)/(steps);
              vpos  = mdvfp+mvpic/2-(i*mvpic)/(2*steps);
            break;
      }

  SEND IIC SETTINGS TO THE SAB9076.THE SETTINGS OF THE FOLLOWING BITS
  SHOULD BE SEND:
  hsize to the bits MHPic
  vsize to the bits MVPic
  hpos to the bits MDhfp
  vpos to the bits MDvfp
 }
```

```
  SWITCH ON THE MAIN PIP
  SEND IIC SETTINGS TO THE SAB9076.
  MHPic
  MVPic
  MDhfp
  MDvfp
}

void ZOOM_MainDown(int Hands[])
{
   int mhpic, mvpic;
   int mdhfp, mdvfp;
   int hsize, vsize;
   int hpos, vpos;
   int hzoom, vzoom;
   int steps;
   int i;

  GET THE IIC DATA FROM THE SAB9076. THE SETTINGS OF THE FOLLOWING BITS ARE
   NEEDED:
  MHPIC
  MVPIC
  MDhfp
  MDvfp

  GET THE DATA FROM THE CONTROL SOFTWARE. THE FOLLOWING DATA ARE NEEDED:
  Zoom on or off.
  The number of stepS
  The direction of the zoom

    for (i = steps-1; i > 5; i--) {
        switch ( hzoom ) {
            case ZOOM_None :
                    hsize = mhpic;
                    hpos =  mdhfp;
                break;
            case ZOOM_Left :
                    hsize = (i*mhpic)/(steps);
                    hpos  = mdhfp;
                 break;
            case ZOOM_Center :
                    hsize = (i*mhpic)/(steps);
```

```
                hpos = mdhfp+mhpic/2-(i*mhpic)/(2*steps);
              break;
        }
       switch ( vzoom ) {
          case ZOOM_None :
                vsize = mvpic;
                vpos =  mdvfp;
              break;
          case ZOOM_Left :
                vsize = (i*mvpic)/(steps);
                vpos  = mdvfp;
             break;
          case ZOOM_Center :
                vsize = (i*mvpic)/(steps);
                vpos = mdvfp+mvpic/2-(i*mvpic)/(2*steps);
              break;
        }
   SEND THE IIC DATA TO THE SAB9076. THE SETTINGS OF THE FOLLOWING BITS
   SHOULD BE SEND:
   hsize to the bits MHPic
   vsize to the bits MVPic
   hpos to the bits MDhfp
   vpos to the bits MDvfp
 }

 SWITCH OFF THE MAIN PIP
 SEND IIC SETTINGS TO THE SAB9076.
 MHPic
 MVPic
 MDhfp
 MDvfp
}
```

10 Application information per pin

This section describes the application aspects of the pins. The component choice is often a compromise and depends on the requirements defined by the customer.

10.1 TM_2, Multistandard or NTSC.

Switch between multistandard and NTSC mode	pins 22

When pin TM_2 is connected to Vss, the SAB9077 is in the multistandard mode.
When pin TM_2 is connected to Vdd, the SAB9077 is in the NTSC mode. This means that the SAB9077 works like the SAB9076

10.2 Memory (external VDRAM) data bus

Data bus from the external memory	pins 23 - 30
Data bus to the external memory	pins 32 - 39
Data bus for memory address and control	pins 31, 39, 46 - 58

All these pins are connected directly to the external memory (VDRAM).

10.3 Test-Mode data bus

Data bus for the test mode	pins 18 -21, 63

This data bus is used for measurements on the device.
These pins should be connected to ground.

10.4 Supply voltages

The supply voltages for the SAB9077 can be divided into:
1. Analog supply voltages
2. Digital supply voltages

The nominal supply voltage is 5.1 Volt

10.4.1 Analog supply voltages

Main analog supply voltages	pin 11, 99
Sub analog supply voltages	pin 70, 82
Display analog supply voltages	pin 83,98

For each analog supply voltage a circuit that stables the supply voltage must be added. The supply voltage namely must be as clean and as stable as possible. The circuit for stabilising and cleaning the supply voltage is shown in picture.

The resistor R=10 Ohm damps changes in the power supply voltage.

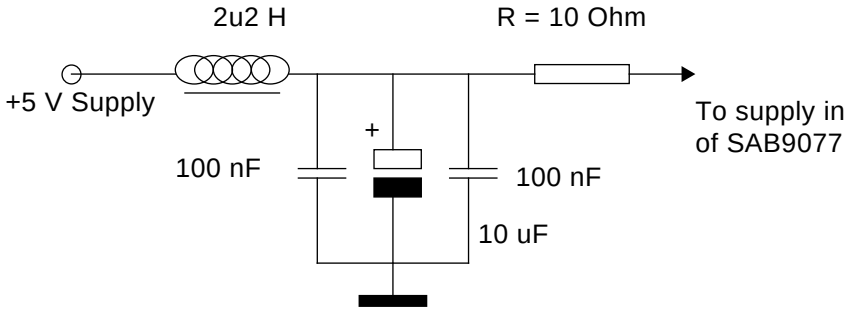


Figure 28: Circuit for stabilizing the voltage for each analog supply pin

10.4.2 Digital supply voltages

Main digital supply voltages	pin 4, 14, 15
Sub digital supply voltages	pin 66, 67, 77
Display digital supply voltages	pin 42, 43, 45, 93

For the digital supply voltages a circuit that stables the supply voltage must be added. The supply voltage namely must be as clean and as stable as possible. The circuit for stabilising and cleaning the supply voltage is shown in picture.

The resistors R=10 Ohm damp changes in the power supply voltage.

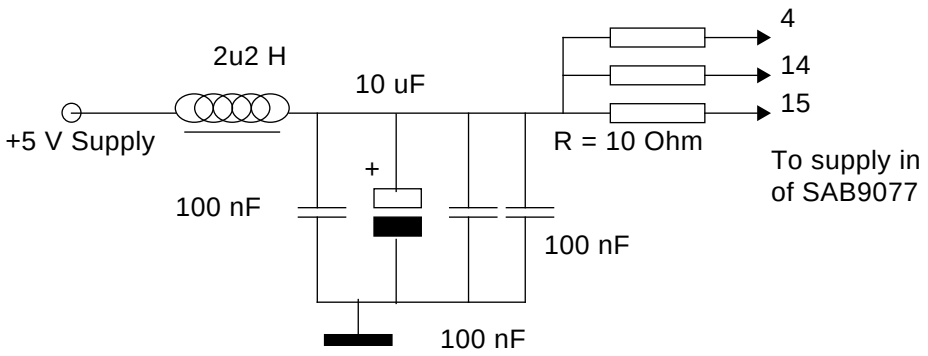


Figure 29: Circuit for stabilizing the voltage for the digital supply pins

10.5 Ground

Grounding	Pins 3, 12, 13, 16, 41, 43, 44, 65, 68, 69, 78, 81, 84, 91, 97, 100

All these grounding pins should be connected to the ground-plain.

The use of a ground-plain is highly preferable to make interference as minimum as possible.

10.6 Luminance input main and sub

Luminance input	Main: pin 10 Sub : pin 71

A video input signal of 1.5 Vpp must be AC coupled to the input pin, with a capacitor of 100 nF.
This capacitor is also used in the clamping circuit. Clamping is done during the burstkey period. The clamping is slow to ensure optimal clamping performance for noisy luminance signals.
The clamp level of the SAB9077 is 0.4 V, is equal to the Vrefb of the ADC.

Because the clamping is done outside the SAB9077, it is advisable to minimize the length of the track between capacitor and luminance input pin.

It is also advisable to make a good ground shielding for the luminance signal track, for good interference immunity.

10.7 Color difference inputs U and V, of main and sub

color difference input U	Main: pin 6 Sub : pin 75
color difference input V	Main: pin 8 Sub : pin 73

The U and V signals are AC coupled via a capacitor of 100 nF
The value of this capacitor can be calculated with the formula:

$$C = i \frac{\partial t}{\partial V}$$

C is the capacitor value.
i Is the output current of the clamp circuit, this is 90 uA
t Is the time in which the capacitor is charged, this is 2.0 uS
V is the maximum deviation in the clamp voltage per line. This value is set to 1.8 mV (= 1/3 LSB).

This capacitor is also used in the clamping circuit. Clamping is done during the burstkey period. The clamping is slow to ensure optimal clamping performance for noisy luminance signals.
The clamp level for the U and V input signals of the SAB9077 is Vreft - Vrefb / 2.

Because the clamping is done outside the SAB9077, it is advisable to minimize the length of the track between capacitor and luminance input pin.

It is also advisable to make a good ground shielding for the luminance signal track, for good interference immunity.

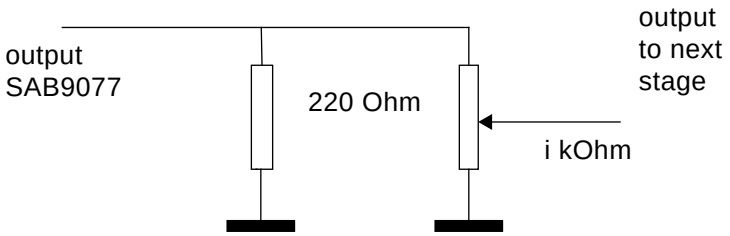
10.8 Output signals of the display part Y, U and V

Output signal Y	pin 86
Output signal U	pin 90
Output signal V	pin 88

The output impedance for the Y, U and V output signals depends on the overall gain wanted. The nominal output impedance, this means the output impedance that causes a overall gain of 1, is 220 Ohm.
With this output impedance the best performance is obtained, because the output swing of the DAC are maximum, and equal to the input range of the ADC.

The minimum load resistance is 75 Ohm.
The maximum load resistance is 10 kOhm.

Another load resistor, which is variable, can be added to the output signals to control the input signal to the next stage of the application. This variable resistor can have a value of 1 kOhm.



10.9 IIC inputs

SDA	pin 61
SCL	pin 60

Both pins should be connected via a 100 Ohm resistor to the controlling device, such as a uProcessor or PC.
The pulses coming from the controller should be 5V pulses, at a baudrate of maximum 400 kHz

10.10 H-sync inputs

V-sync inputs for main-, sub- and display channel pin 2, 79, 95

All three pins are directly connected to the decoding device, such as the TDA8315 or TDA8310.
The H-sync or burstkey signal should be a normal 5 V pulse, of which the rise- and fall- time should be as small as possible (<<100 nS).
Both flanks should be clean, that means free from noise, ringing etc.

10.11 V-sync inputs

V-sync inputs for main-,sub- and display channel pin 17, 64, 94

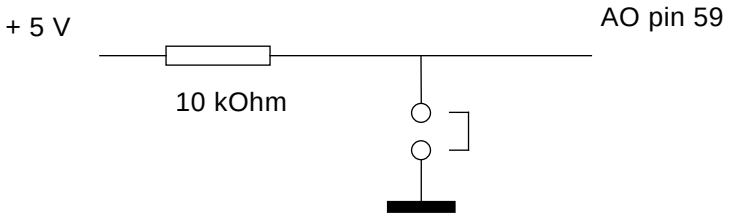
All three pins are directly connected to the decoding device, such as the TDA8315 or TDA8310.
The V-sync signal should be a normal 5 V pulse, of which the rise- and fall- time should be as small as possible (<<100 nS).
Both flanks should be clean, that means free from noise, ringing etc.

10.12 IIC-Address input

IIC-address pin AO pin 59

Pin AO is used to select the IIC address of the SAB9077.

pin AO = 0 V IIC address is 2C H
pin AO = +5 V IIC address is 2E H



10.13 ADC reference signals

Vbias main and sub pin 5, 76
Vreft main and sub pin 7, 74
Vrefb main and sub pin 9, 72

all these pins need a capacitor for decoupling.
The reference voltage is made internally in the SAB9077 from the analog supply voltage. A stable and clean supply voltage is very important.

The value o the capacitor should be 100 nF, and it should be placed as close as possible to the reference pins.

10.14 Power on reset

power on reset pin 62

Some digital blocks inside the SAB9077 need to be resetted, before the SAB9077 can work properly. After power down these digital blocks can still contain data. If the device is switched on, these data can bring the SAB9077 into an unstable mode.
To avoid an unstable mode after power up these digital blocks have to get a reset signal. The power on reset pin generates the reset signal.

After power up the capacitor connected to pin62 will be charged, and the reset pulse will be generated by the inverter.
If the voltage on pin 62 becomes higher than 3.5 V, the reset pulse will disappear and the SAB9077 will start up.
The power on reset delays the start up of the SAB9077.

The only restriction to the value of the capacitor is that the rise time on pin 62 should be longer than the rise time of the supply power. The value of the capacitor should be > 100 nF.
Recommended value of the capacitor is 1 uF.

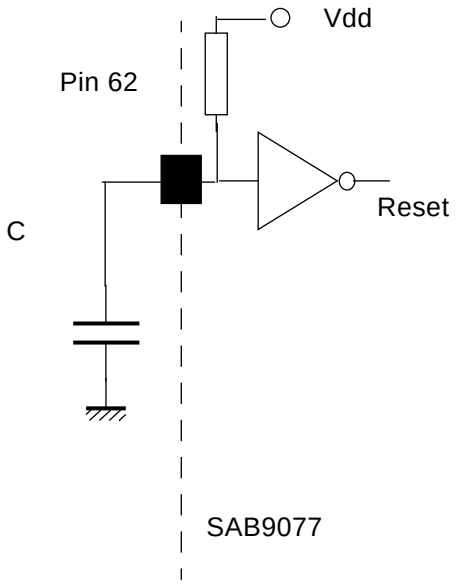


Figure 30: Power on reset circuit

If the power on reset pin is also connected to the uProcessor, power dips at the SAB9077 board can be detected. After a power dip all registers of the IIC-bus are filled with 00 H, so the IIC data should be send to the SAB9077 once again to keep the selected mode running.

10.15 Fast blank DFB

Fast blank pin 93

This pin is the output pin of the fast blank signal. The fast blank signal determines the place where in the original live picture a cut out will be made. The space in this cut out will be filled with the PIP pictures.

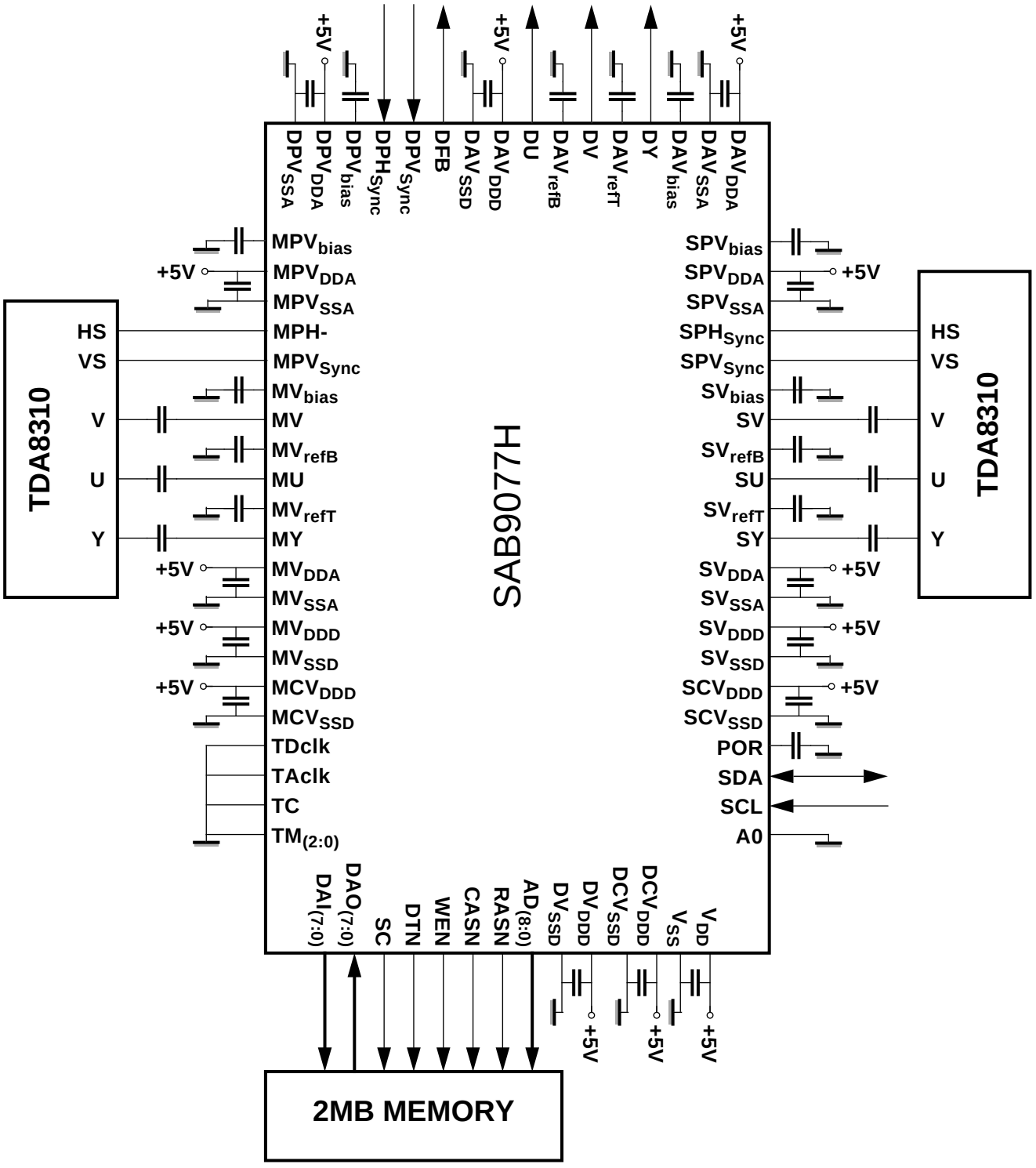


Figure 31: Application diagram of the SAB9077H

In Figure 31 the application diagram of the SAB9077H is depicted for use with the TDA8310A. All capacitors are 100 nF. On the application board a ground plane should be used.